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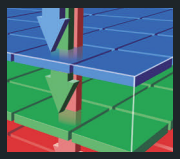
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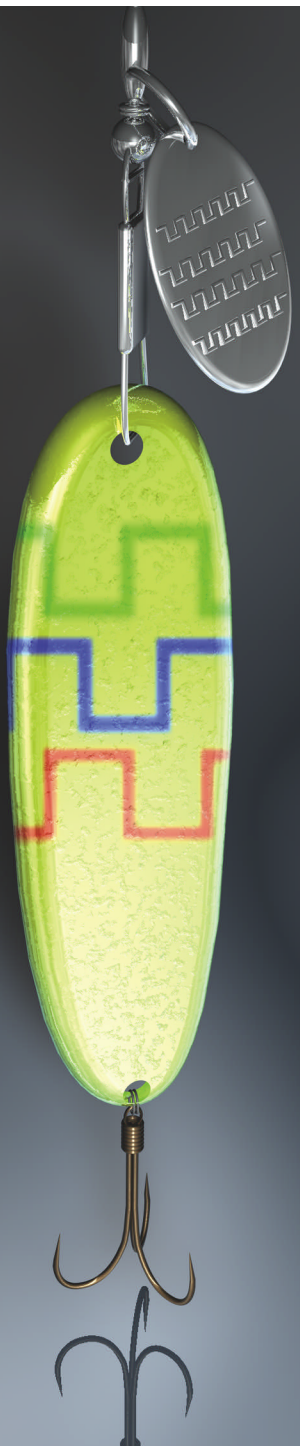
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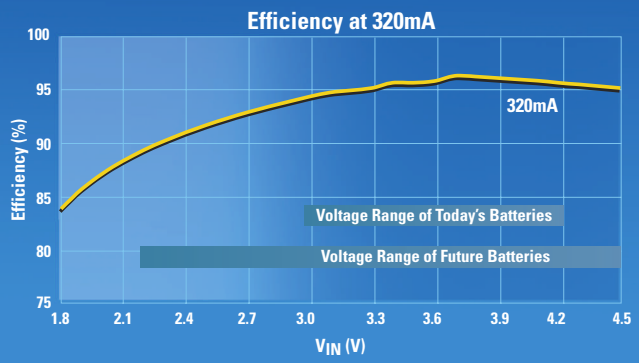
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Longer Run-Time

96% Efficient Buck-Boost Converter

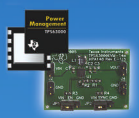
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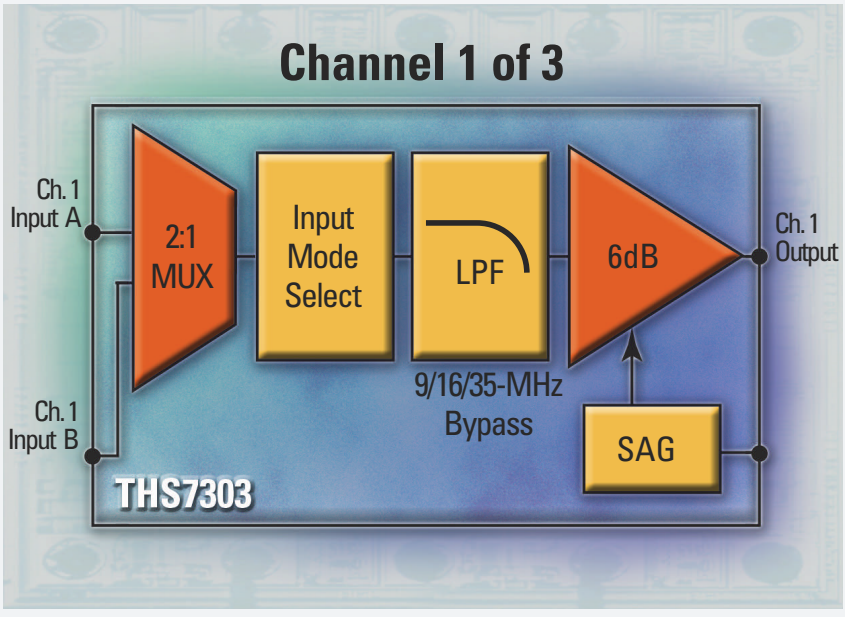
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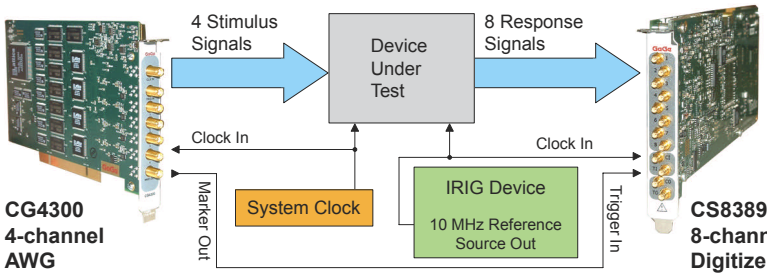


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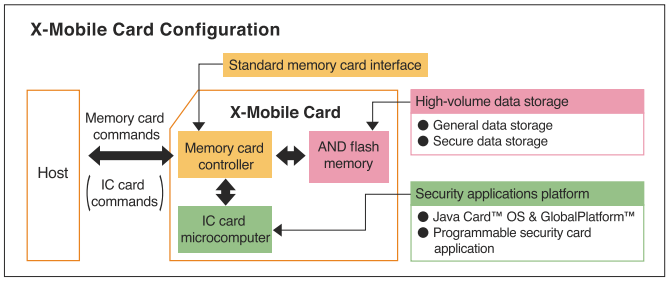
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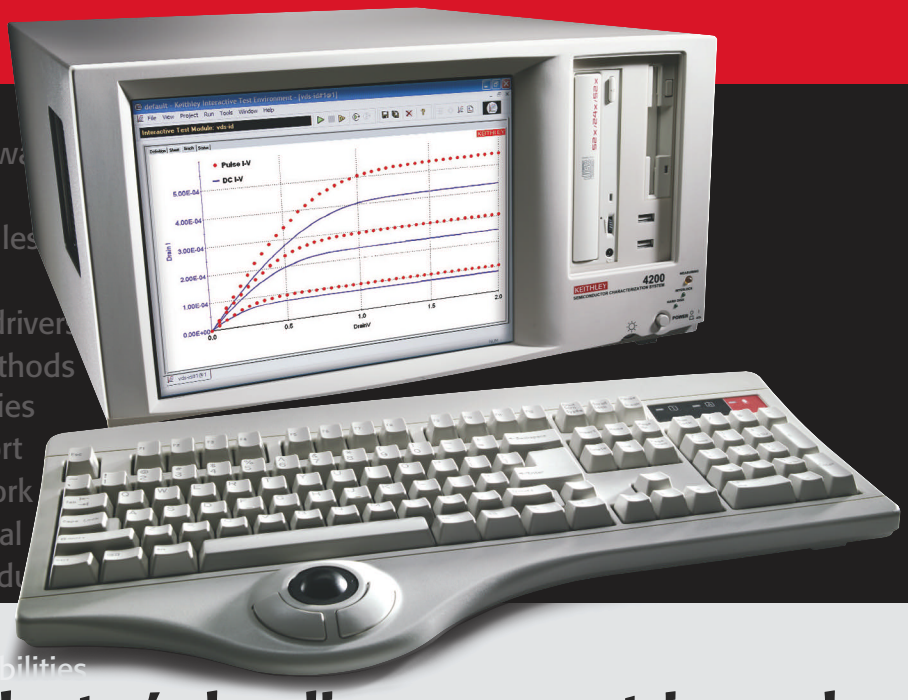
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Digital power lures system architects, power-supply vendors

46 Digital power promises to lower overall system-power costs by improving maintenance costs and reliability, lowering power-component costs, and simplifying BOMs. To achieve these goals, designers must add smarts to the traditionally dumb power subsystem. Digital-power-control and -management ICs offer help.
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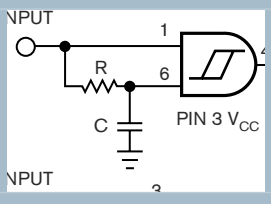
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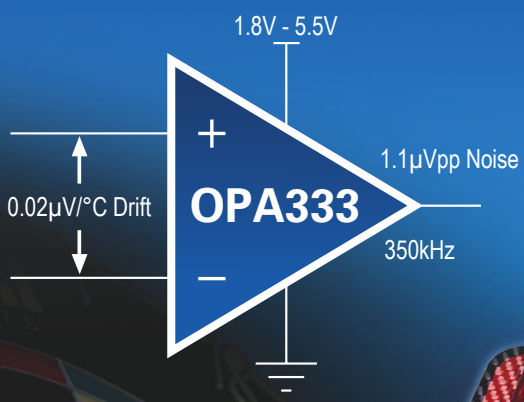


91 JFET-based dc/dc converter operates from 300-mV supply
94 Configurable logic gates' Schmitt inputs make versatile monostables
98 Stealth-mode LED controls itself
100 Data-acquisition system captures 16-bit voltage measurements using the USB

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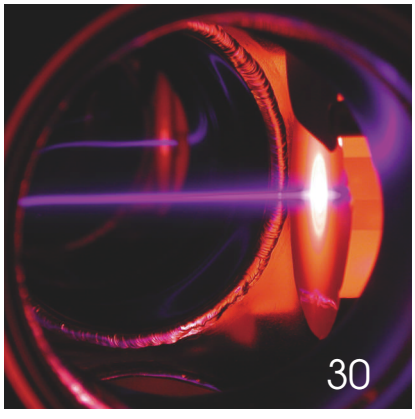
24 Real-time-DSO bandwidth reaches 18 GHz—fast enough for 10-Gbps data streams

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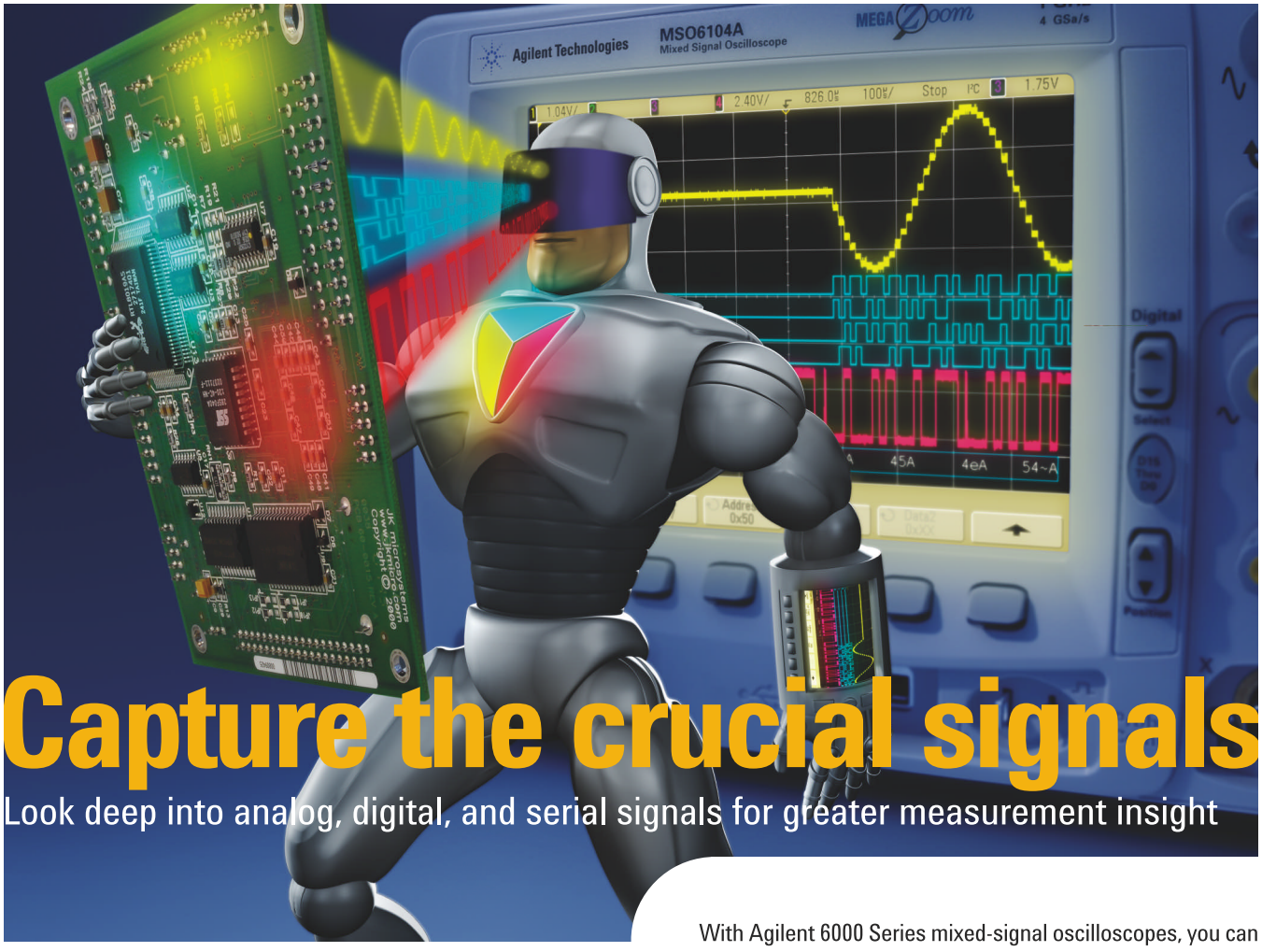
PRODUCT ROUNDUP

105 **Power Sources:** Lithium-ion-charger chips, dc/dc converters, PFC controllers, buck-voltage regulators, and more

109 **Test & Measurement:** Spectrum analyzers, debugging devices, and more

110 **Integrated Circuits:** Audio DSPs, system on chips, image sensors, frame-rate-converter ICs, quad-channel decoders, and more

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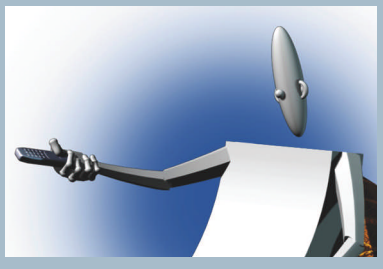
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IN CELEBRATION OF OUR 50TH YEAR OF PUBLICATION, we're revisiting articles from deep in the *EDN* archives in a new department called Milestones That Mattered. In each installment, we analyze an event that turned out to have lasting significance—even if no one (including *EDN* editors) grasped its importance at the time. Read the latest Milestones That Mattered column on pg 36 and check out these previous editions:

The planar IC—revolution underestimated (April 27, 2006)
Read *EDN*'s 1960 coverage of the development of the planar IC. We underestimated its importance—but so did everyone else.
→www.edn.com/article/CA6325586

RAMAC launched disk-drive revolution (March 30, 2006)
A two-paragraph item in the November 1956 issue of *EDN* noted IBM's development of the 350 Disk File, precursor to today's hard-disk drives.
→www.edn.com/article/CA6317063

FROM THE VAULT

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DIGITAL POWER LURES SYSTEM ARCHITECTS, POWER-SUPPLY VENDORS (pg 46):

Digital power IC combines power conversion and management
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Digital power controller is fast and software-configurable
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SCALING: A BALANCED VIEW, PART TWO (pg 34):

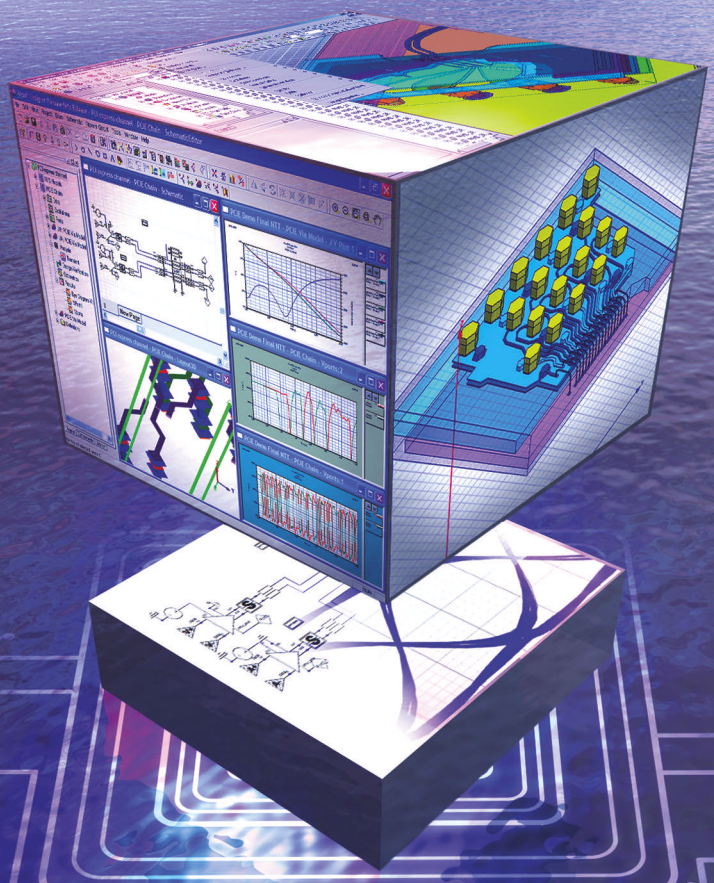
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Baker's Best: Three alternatives to your aliasing problems
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BY MAURY WRIGHT, EDITOR IN CHIEF

The PC is the workstation

Is the specialty-engineering workstation dead? Just this morning, I read that Silicon Graphics (www.sgi.com) filed for Chapter 11 protection (**Reference 1**). The account blamed the company's troubles in part on "competition from machines based on standard components used in PCs." This news came just two weeks after Scott McNealy stepped down from his post as chief executive officer of Sun Microsystems (www.sun.com). And Sun's business in both workstations and servers has for several years fared poorly. Without question, the PC is behind the trouble at both companies. But just how did the PC displace the workstation?

In December 1998, I did a hands-on comparison of Windows NT-based PCs and Unix workstations (**Reference 2**). I tested systems ranging from a Pentium II PC that I built to a Compaq (www.compaq.com) dual-processor Pentium II-based workstation to a Hewlett-Packard (www.hp.com) J Class Unix workstation. The PCs fared well, although the larger caches in the Unix systems paid off in some applications. But, at the time, readers were adamant that engineering work demanded a Unix workstation. The readers based their preference on the operating system rather than on the hardware. A column in the same issue stated my preference for Windows NT over Unix (**Reference 3**). It garnered a response from readers that filled my e-mail inbox with a collective critique of my intellect. But I was correct in my prediction that the PC market would supersede the workstation market.

Since 1998, many factors have combined to undermine the future of the specialty workstation. First, workstations lost whatever performance edge they once held. The effort of HP and Intel (www.intel.com) to build the Itanium processor has been a failure in workstations and has fared only slightly better in servers. Sun has also failed to offer compelling performance advantages in UltraSPARC. In fact, Fujitsu (www.fujitsu.com) largely outpaced Sun in UltraSPARC development, even though Sun used its own Texas Instruments (www.ti.com)-manufactured chips. But the availability of Pentium-class designs from both AMD (www.amd.com) and Intel has erased any advantage that UltraSPARC once enjoyed. The features of PC-support chips, such as graphics processors from Nvidia (www.nvidia.com) and ATI (www.ati.com), have also equaled or surpassed the abilities of mainstream workstations.

Linux is the second factor in the success of the PC as a workstation. I was wrong in 1998 about Windows NT. Even today, Windows XP lacks the robustness for critical engineering applications. But major EDA companies have ported their applications to Linux. Sun and others have always made many of their profits from their operating systems and were slow to embrace Linux. But that latency cost them hardware business in both workstations and servers.

Finally, notebook technology has made PC workstations popular with engineers. Today, engineers can take their workstations home or on trips, and those workstations are still fairly powerful tools. Several companies once tried to roll out portable Unix workstations, but the technology was expensive and never caught on. But the skyrocketing popularity of notebooks has led to amazing developments in power-system design, cooling, and low-power ICs that allow notebook vendors to offer systems that approach the power of a desktop. Gaming notebooks are among the hottest segments and offer the performance and graphics features—albeit with a different operating system—that design engineers need.

With the workstation and server segments vulnerable, Sun, Silicon Graphics, and others have fallen back on the high-performance-computing segment. The companies offer densely clustered systems and even supercomputers. But PC hardware is also attacking the high-performance-computer market. The Top 500 Supercomputer Sites Web page lists the most powerful systems (**Reference 4**). A system based on Dell (www.dell.com) PowerEdge systems occupies the fifth spot.

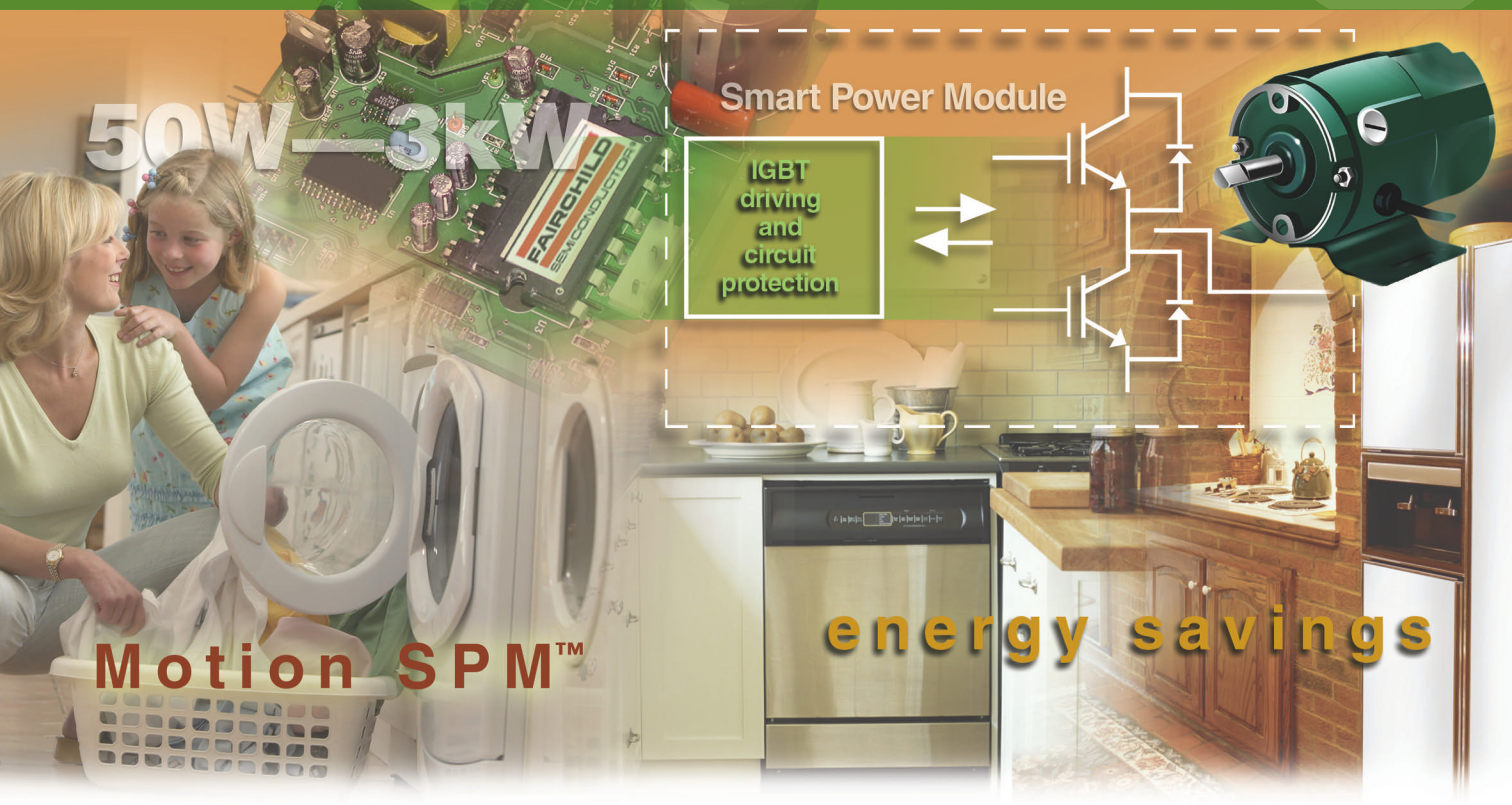
When I consider the success of the PC in the high end, the continued push into multiple-PC homes, and the Trojan-horse approach to hiding PCs inside PVRs (personal video recorders) or next-generation HD-DVD players, I have to wonder about those people who claim that the PC is dead. How could we live without the PC, whose success underlies everything from test equipment to industrial control to automotive systems? EDN

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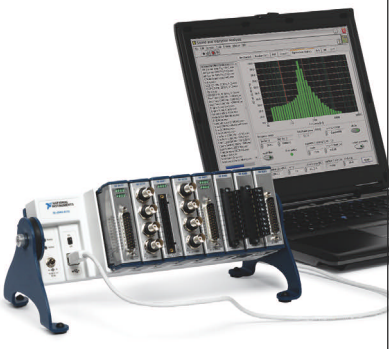
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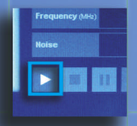
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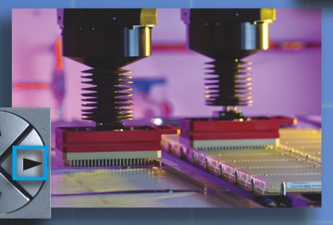


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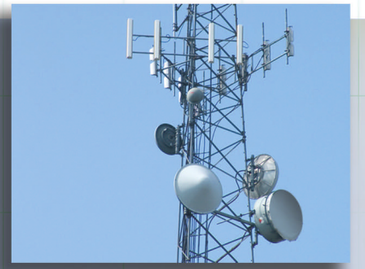
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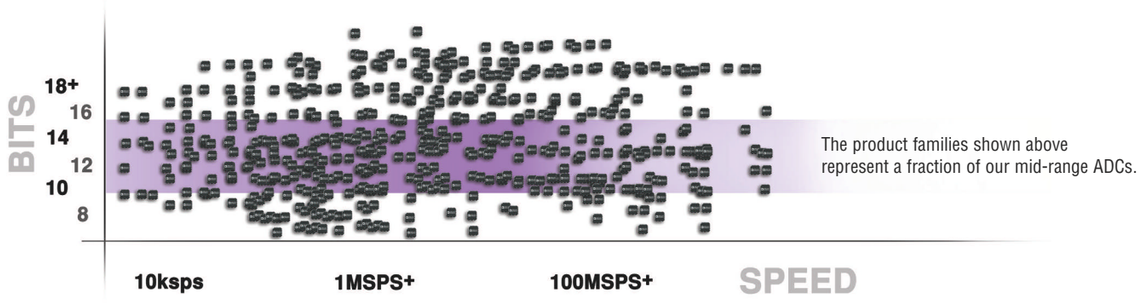


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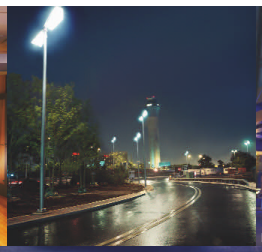


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USB 2.0 becomes interface to modular data-acquisition systems

Although USB has become popular as an interface for small, stand-alone, multichannel data-acquisition units, National Instruments' announcement of the CompactDaq system adds another dimension—plug-in modularity—to USB-based data acquisition. Many sensors require excitation, signal conditioning, or both, and many instrumentation setups use multiple sensor types that require different kinds of signal conditioning. A system might include several dc-excited, strain-gauge-bridge-based load cells; several piezoelectric accelerometers; and a few thermocouples. Without additional hardware, stand-alone USB data-acquisition units can't handle such combinations.

The 2.75×3.44×0.875-in. C-series I/O modules, which sell for $12 to $325 per channel, not only handle the signal conditioning and analog-to-digital conversion, but also provide appropriate physical interfaces, such as screw terminals or connectors, for the sensors.

The series currently includes 11 types of modules, several of which handle multiple channels. Eight modules fit into a 10× 3.47×3.47-in., 11 to 30V-dc-powered CompactDaq chassis. One of the modules accepts 32 analog inputs, allowing one chassis to monitor 256 channels. For applications that require ac-line power, NI provides an external ac-to-dc supply. Depending on the module type, ADC resolution is either 16 or 24 bits. Analog-to-digital-conversion rates range from 15 samples/sec to 250k samples/sec. Speed of the digital-I/O channels is 10 MHz. The system interface is high-speed USB 2.0.

—by Dan Strassberg

▷**National Instruments**, www.ni.com.



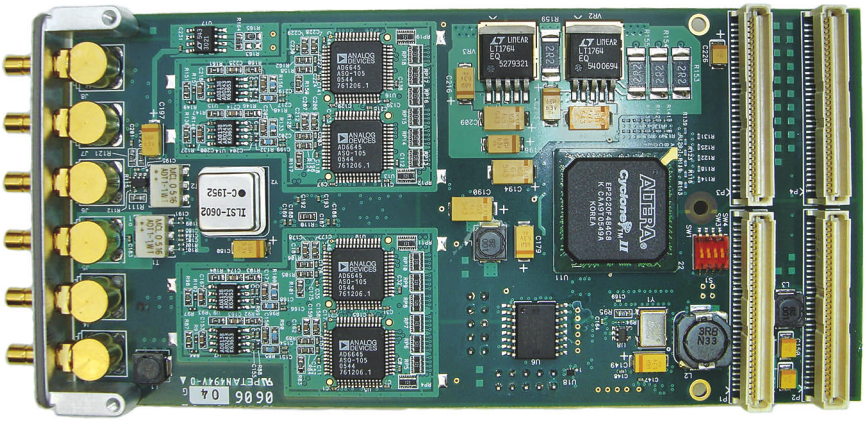
CompactDaq systems bring modularity and ease of connection to USB-based data acquisition.

PMC board unites four ADC channels, FPGA

BittWare recently announced a high-performance analog-to-digital-I/O card in the PMC (PCI-mezzanine-card) form factor. The high-speed TRPM+ (Tetra-PMC+) analog-input board provides data capture for four 14-bit ADC channels operating as fast as 105 MHz and streams this data directly to a reconfigurable Altera (www.altera.com) Cyclone II FPGA. The FPGA controls the ADCs; distributes the high-speed, converted data; and enables configurable preprocessing of the data for digital filtering, decimation, and digital downconversion.

BittWare offers software-development tools that allow designers to develop application code and integrate the Tetra-PMC+ into their systems. For user-configured preprocessing, Altera provides a suite of development tools for the Cyclone II. The TRPM+ will be available in the second quarter of this year at a list price of $3995.**—by Warren Webb**

▷**BittWare Inc**, www.bittware.com.



The Tetra-PMC+ board features four ADCs operating as fast as 105 MHz and a Cyclone II FPGA providing control, data distribution, and front-end processing.

New HyperTransport version opens multicore doors

HyperTransport, the physical-layer interchip-communications standard whose claim to fame has been its use on Advanced Micro Devices (www.amd.com) CPU chips, has rolled out its most recent revision, HyperTransport 3.0. The new spec substantially changes the capabilities of the interface, broadening its applicability and positioning HyperTransport as a foundation technology for the future of board-level multiprocessing.

Fundamentally, HyperTransport has been an elegantly simple concept: 16 data lines plus clock-signal and sideband-control-signal pins, all running synchronously using LVDS (low-voltage differential signaling). Running at a 1.4-GHz clock rate, the 2.0 version of the specification offered both high peak data rate and low latency, which are important for the short-haul, chip-to-chip backbone applications that it targets. As a thin, point-to-point-interconnect layer, HyperTransport can power up, transfer a string of packets, and power down with nearly as little fuss as simple point-to-point wiring but at much higher speeds than would be possible for individual asynchronous links.

This virtue led to AMD's decision to adopt HyperTransport for inclusion on the company's recent CPU designs, serving as the link between the CPU and the north bridge and, more significantly for the future, the link between CPUs, both on the die in the dual-core Opteron and between chips in board-level multiprocessing servers. AMD also uses the link to connect accelerator cores to CPUs.

The most obvious difference between 3.0 and 2.0 is the 3.0's higher maximum clock speed: 2.6 GHz. This increase allows aggregate throughput over a 16-bit link of 20.8 Gbytes/sec. This change, in turn, demands increased complexity on both the transmitter and the receiver sides of the connection. The transmitter gets enhanced training patterns to cope with the multibit skew that can occur at these speeds. It also now can employ scrambling to ease the receiver's recovery job. The receiver has added equalization capabilities and can use clock-based phase alignment to undo multibit skew in the interconnect medium. Along with these new features, the new version retains 100% compatibility with previous operating modes.

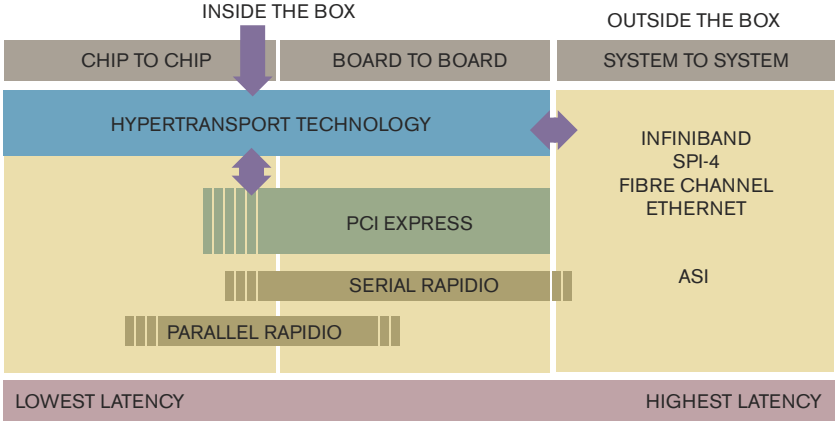
The 3.0 specification also retains HyperTransport HTX—the ability to operate at longer distances and through a standard connector. This feature permits designers to create a HyperTransport link to a daughtercard, allowing plug-in accelerator cards. The spec also retains a hot-swapping feature with a nod toward the online-maintenance needs of server farmers.

These features also have demanded new technology at the higher clock rate. Under the new standard, a HyperTransport interface must sense when it is capacitively coupled to its partner through an HTX link, as opposed to directly wired to the partner through a standard chip-to-chip link. If the HTX link is in use, the interface must shift to an 8b/10b-coding scheme. This requirement means that the receiver must execute a more complex clock-recovery algorithm.

Concurrently with the release of the specification, the HyperTransport Consortium has announced that GDA Technologies (www.gdatech.com) is developing HyperTransport 3.0-interface IP (intellectual property). Extensive discussions have taken place with AMD—a major player in the new spec—and with accelerator vendors and FPGA leaders.

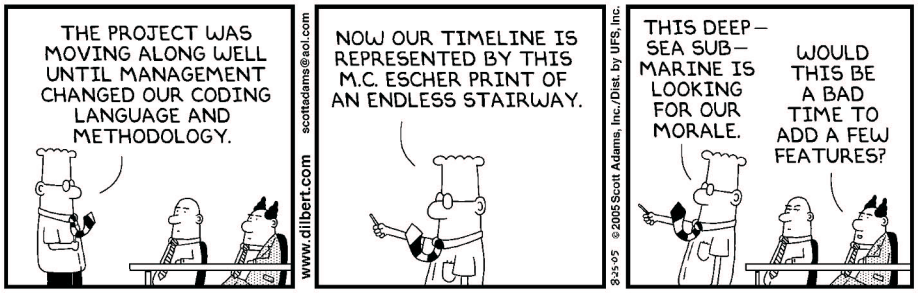
—by Ron Wilson

▷**HyperTransport Consortium**, www.hypertransport.org.



The latest version of HyperTransport substantially changes the interface.

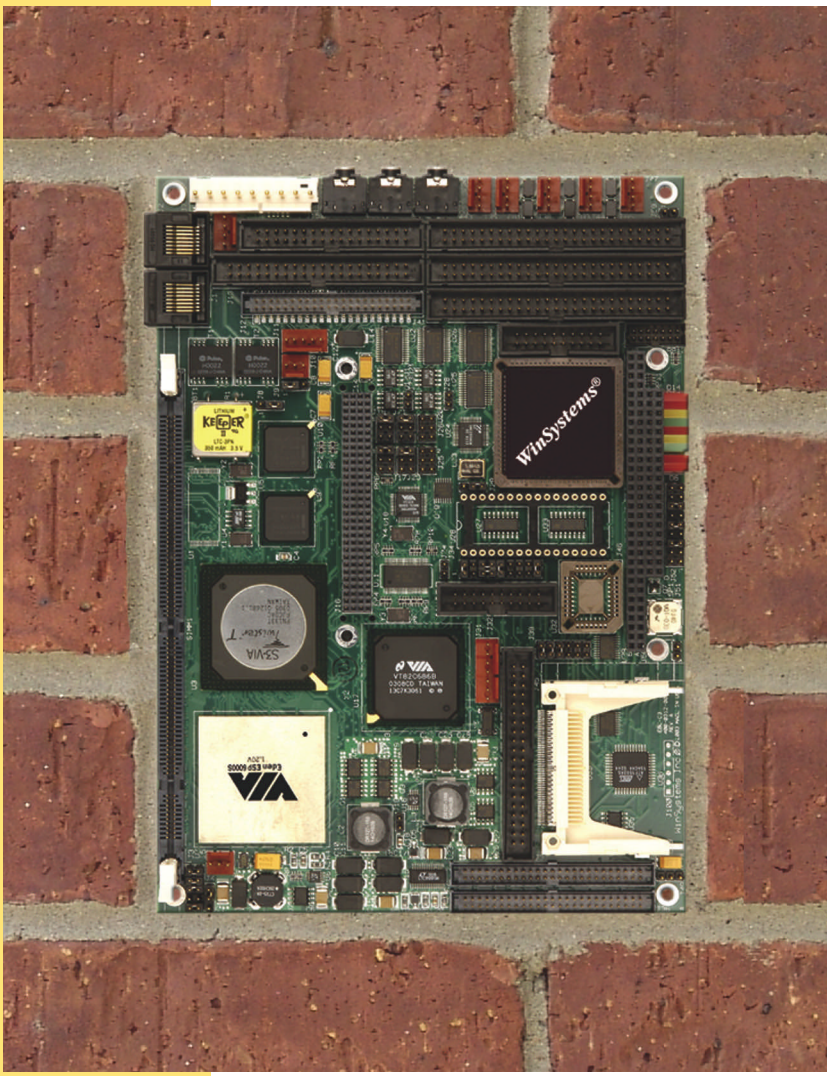
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Real-time-DSO bandwidth reaches 18 GHz—fast enough for 10-Gbps data streams

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Although the scope has four channels, you can obtain the high bandwidth on only one. Moreover, when you use the 18-GHz mode, the only other usable channel offers bandwidth of only 6 GHz. You can also select 11-GHz bandwidth on one channel and 6 GHz on two channels or 6 GHz on all four channels.

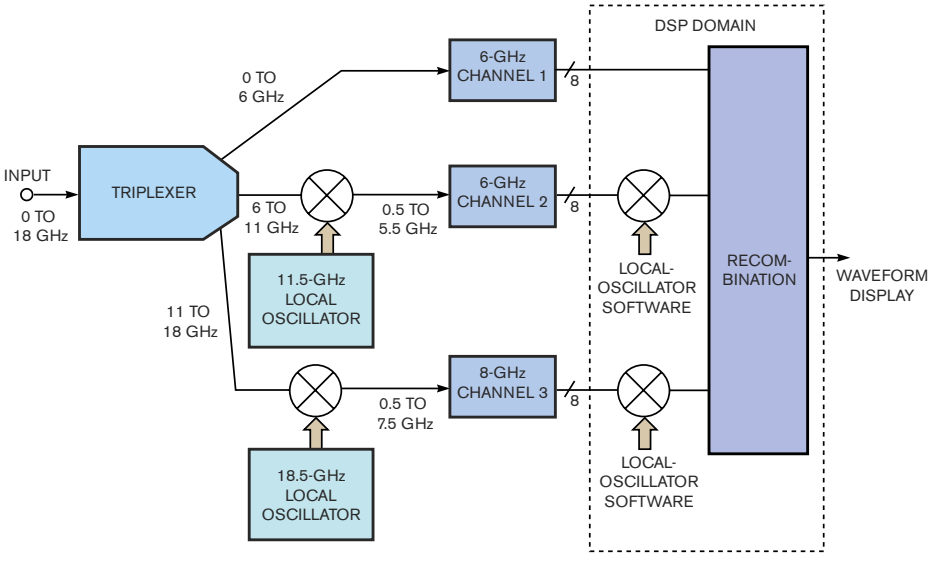
Unlike the other two real-time scopes that offer bandwidth greater than 12 GHz, the SDA 18000 does not enhance its bandwidth by using digital-signal processing, an approach that LeCroy says presents some significant drawbacks, including waveform distortion and increased baseline noise. The excessive noise can lead to a scope's reporting erroneously high jitter on signals under test. A scope can, however, also use digital-signal processing to reduce its noise. According to LeCroy, the SDA 18000 and at least one competitive scope use this approach. But using digital-signal processing both to enhance bandwidth and to reduce noise results in noise greater than that obtainable in a scope that uses digital-signal processing only to reduce noise.

LeCroy achieves the 18-GHz bandwidth through a technique it calls DBI (digital-bandwidth interleaving). To amplify an 18-GHz-bandwidth signal, the SDA 18000 uses two amplifiers with a −3-dB bandwidth of 6 GHz and one with a bandwidth of 8 GHz. One amplifier processes the portion of the signal that extends from dc to 6 GHz. A second amplifier, preceded by a mixer and a downconverter, mixes an 11.5-GHz carrier with the portion that extends from 6 to 11 GHz to translate its frequency range downward to 0.5 to 5.5 GHz. The scope then amplifies and remixes this amplified signal with the 11.5-GHz carrier for upconversion back to the 6- to 11-GHz band. A similar approach subtracts 18.5 GHz from the 11- to 18-GHz portion of the signal, amplifies it, and upconverts it to its original frequency band. The 6-, 5-, and 7-GHz-bandwidth signals then recombine to produce a single amplified, 18-GHz-bandwidth signal. Three time-interleaved, 20G-sample/sec ADCs then digitize the signal, producing a single digitized record of the 18-GHz-bandwidth signal.

> When you operate the channels separately and the scope is digitizing at its maximum rate, the three ADCs make simultaneous conversions every 50 psec.

When you use the scope as a four-channel, 6-GHz-bandwidth instrument, it redeploys the 6- to 11-GHz amplifier and one of the ADCs and its associated acquisition memory to Channel 2 and the 11- to 18-GHz amplifier and its ADC and acquisition memory to Channel 3. This mode does not use the two mixers from Channel 2, the two from Channel 3, or the final mixer. In addition, when you operate the channels separately and the scope is digitizing at its maximum rate, the three ADCs make simultaneous conversions every 50 psec, whereas, in the interleaved mode, the conversion duties rotate among the three ADCs. Every 16.67 psec, one of them digitizes the 18-GHz-bandwidth signal.

Another feature of the SDA 18000 is its use of a Q-Scale feature for jitter analysis. LeCroy believes that its new scope is the first to offer this feature, but the company expects that at least one of its competitors will soon offer the



Using digital-bandwidth interleaving, the SDA 18000 uses three amplifiers to amplify 5-, 6-, and 7-GHz segments of an 18-GHz-bandwidth signal. The scope then reassembles the signal into an amplified replica of the original, and three time-interleaved, 20G-sample/sec ADCs digitize it.

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Transmit eye diagram at 6.375 Gbps. For characterization details, see www.altera.com/stratix2gx/characterization.

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feature. Q-Scale replots the envelopes of gaussian jitter distributions as straight lines, enabling you to more quickly determine peak-to-peak jitter and to easily separate random and deterministic jitter components.

As you might expect, the high bandwidth comes at a premium; the base price is $128,000. However, when you order the scope with a new, 18-GHz differential amplifier and software that decodes the 8b/10b embedded clocking in ultrahigh-speed data streams, the price comes to $144,490. An option that increases the per-channel memory to 16M points (48M in the 18-GHz mode) costs $4990, and an option that increases the per-channel memory depth to 50 million points (150 million in the 18-GHz mode) costs $14,990. Note that, at the 60G-sample/sec acquisition rate in the 18-GHz mode, the duration of a 150-million-point record is only 2.5 msec. Owners of LeCroy's earlier SDA 11000 scopes can trade up to the SDA 18000 for $86,000.

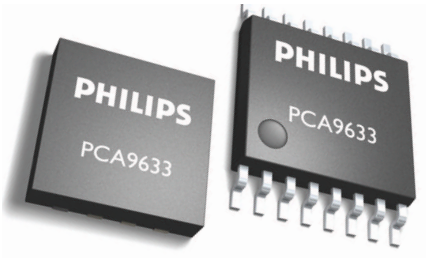
For those who can get by with 9-GHz bandwidth, LeCroy is introducing the SDA 9000 with prices starting at $90,000. This unit also has four channels, which, when you use them separately, each provide a bandwidth of 6 GHz. However, the unit has no 18-GHz mode. Instead, you can operate the scope with two 9-GHz-bandwidth channels or one 9-GHz channel and two 6-GHz channels. Prices for the SDA 9000 with deep memory are the same as those for the SDA 18000.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.

Serial bus enhances venerable I²C-bus speed

Since Philips in the early 1980s developed the I²C as a two-wire, low- to medium-speed communication bus, it has become the de facto standard for onboard communication and, when you bolster it with drivers, for board-to-board communication. However, as communication speeds have increased and interboard and even intercabinet communication have become commonplace, the I²C bus has been in need of a speed and drive-capacity overhaul. Hoping to bring users up to date and attract a new user base, Philips has now introduced a family of devices based on the Fm+ (fast-mode-plus) specification. Fm+ tightens the bus tolerances and timing requirements and allows a top speed of 1 MHz versus 400 kHz for the old version and a 10-times-greater-than-normal bus-drive capability of as much as 4000 pF.



Fm+ tightens the bus tolerances and timing requirements and allows a top speed of 1 MHz versus 400 kHz for the old version and a 10-times-greater-than-normal bus-drive capability of as much as 4000 pF.

"Most of our customers needed to make trade-offs between the bus length, the speed, and the number of devices on the bus," says Dhwani Vyas, general manager of the interface-product line at Philips Semiconductors. "Fm+ gives a larger playing field: With fewer devices, you can go longer distances." The new specification also allows for device ID, which allows you to query each device about its manufacturing and revision-level information. In addition, Fm+ allows for three address pins on each device with four states, allowing for as many as 64 device addresses.

"Fm+ is an extension of the I²C spec," says Steve Blozis, marketing manager for I²C-logic devices at Philips. "The devices will be backward-compatible with I²C buses." According to Blozis, some backers of other buses similar to I²C, such as the SMBus, have been concerned because Philips owned a patent on the bus, but the basic I²C patent expired August 2004.

The initial three devices in the new family are the PCA9633 4-bit I²C LED controllers for RGBA (red-green-blue-alpha) color mixing, the PCA9698 advanced 40-bit I²C I/O expander, and the PCA9665 fast-mode-plus-parallel-bus-to-I²C-bus controllers. Prices range from 55 cents to $2.05.

—by Margery Conner

▷**Philips Semiconductors**, www.semiconductors.philips.com.

USB power manager integrates battery charger

05.25.06

Designing the power portion of portable USB-based devices gets easier with the Linear Technology LTC4089 and LTC4089-5. The products integrate battery chargers—the 4089 with a fixed 5V output and the 4089-5 with a variable output that tracks the battery voltage for improved efficiency.

The controller offers a seamless transition between battery, USB, and external 6 to 36V power sources. A 200-mV integrated ideal diode and the integrated optional external ideal-diode controller provide a low-loss power path for battery operation.

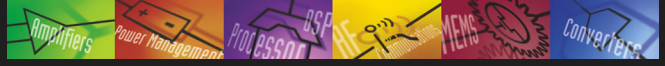
—by Maury Wright

▶**Linear Technology**, www.linear.com.

FROM THE VAULT

"We've come very close to realizing the vision of Teilhard de Chardin: a web of intelligence surrounding the earth, a collective human consciousness with access to all knowledge. This could be the single most important outcome of the communications revolution."

Hal Hellman, heralded science writer, *EDN*, Oct 14, 1981



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ANALOG DEVICES

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GLOBAL DESIGNER

Japanese power-supply vendors see engineers as competitive advantages

Are you feeling a twinge of fear about all those well-educated Chinese engineers who may right now be working on a design that competes with your company's product? Warnings in the business and trade media are currently bombarding engineers in the United States and Europe that well-educated, relatively low-paid Chinese engineers present a seemingly insurmountable threat to their US and European livelihoods. Consider how some Japanese companies have successfully responded to the same threat.

Now a bastion of quality engineering, Japan was a generation ago firmly ensconced in the high-volume, low-margin end of the business spectrum, the traditional way for a cheap-labor country to enter the world market. However, part of the package deal of success is that wages of both professional and unskilled workers rise, and, if cheap labor is the only advantage a country has, it's in danger from the next upstart region.

Many US power-supply vendors fixate on the low-end, cost-driven portion of the power-system business and exhibit lukewarm interest in and commitment to developing digital-power technology for future designs. The most common refrain is that price drives the power-supply business and that any technology that adds to the cost of a power supply can kill the product's competitiveness.

On the other hand, a Japanese power-supply vendor, such as Lambda/TDK, supports three digital-power R&D efforts in three divisions. According to Hiroyuki Yashiro, chief technology officer for Lambda/TDK, the company assumes that, within three years, digital-power technology will play a significant role in the company's products. And Bellnix, a relatively small Japanese vendor of point-of-load converters, a notoriously cutthroat market, is now selling digital-power-technology-based converters. These companies realize that their futures lie in high-end designs for the noncommodity markets. If they rely on bare-bones designs with little added engineering value, Chinese vendors will outsell them.

Why can't China duplicate Lambda/TDK's know-how in switching power supplies, as it has in consumer markets, such as cell phones? Says Takeo Suzuki, president of Lambda/TDK, "Chinese companies have been successful in competing in the cell-phone market because they can easily buy the enabling technology, such as special-purpose processors, from Silicon Valley. That's not the case in high-end-power-supply design. The know-how resides in Lambda's engineers."

—by Margery Conner

▷**Lambda/TDK**, www.tdk.co.jp.

▷**Bellnix**, www.bellnix.com.

Frequency-agile WiMax transceiver matches client to band

Flexibility in frequency band is a big obstacle in WiMax deployment and is also the reason that the wireless-broadband technology can work in any region worldwide. Such flexibility, however, can result in the need for multiple radio implementations for client designs. Belgium-based AsicAhead believes that it can overcome that obstacle with its new, reprogrammable AA1001 transceiver that works across all frequency bands for the IEEE 802.16e mobile flavor of WiMax. The company also claims that the AA1001 design eliminates the need for expensive SAW (surface-acoustic-wave) filters and a TCXO (temperature-compensated crystal oscillator)—components that competing transceivers commonly require. Production quantities are due in the next quarter at $18 (10,000).**—by Maury Wright**

▷**AsicAhead NV**, www.asicahead.com.

Germanium boosts thermophotovoltaic efficiency

Whereas photovoltaic cells directly convert light to electricity, thermophotovoltaic cells rely on light to drive a heat absorber and then convert the heat to electrical energy. The Belgian-based IMEC (Interuniversity Microelectronics Center) lab has developed a new germanium-based process that offers better efficiency than silicon-based thermophotovoltaic cells. Generally, thermophotovoltaic cells benefit from using a material with a lower bandgap than silicon. Germanium meets the bandgap requirement but presents a challenge in surface passivation. IMEC worked with germanium-wafer vendor Umicore (www.umicore.com) to attack the passivation problem because germanium is lower in cost than alternative low-bandgap materials.

The new process forms the shallow emitter of the germanium cell using diffusion from a spin-on oxide. Meanwhile, a thin, plasma-deposited, amorphous silicon layer solves the passivation problem. The result is a cell with an open-circuit voltage higher than 270 mV, an air-mass-1.5-spectra standard efficiency of nearly 8%, and a broad spectral response of 400 to 1700 nm. IMEC claims that the performance significantly exceeds that of cells under the given illumination conditions.

IMEC hopes to move quickly in realizing production of germanium-based cells. The manufacturing process is largely compatible with the organization's solar-cell process, but the cells require refining for stability for use with higher intensity light.—by Maury Wright

▶**IMEC**, www.imec.be.

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RESEARCH UPDATE

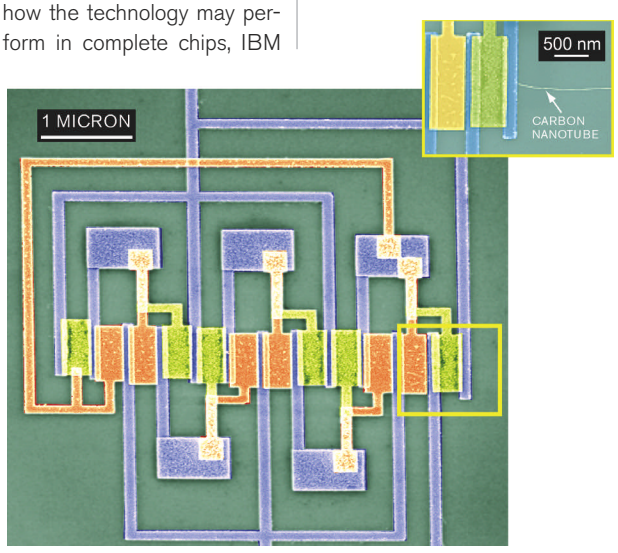
BY MATTHEW MILLER

Scientists complete carbon-nanotube circuit

IBM Research has announced what it claims is the first complete IC built on a single carbon-nanotube molecule. The feat represents a significant advance, according to the company, because it will allow researchers to evaluate the presumed performance benefits of carbon nanotubes over traditional semiconductors.

The IBM scientists built the circuit, a ring oscillator, using standard semiconductor processes and employed a single molecule as the base for all the circuit's components. The architecture uses unique carbon-nanotube properties and maintains compatibility with established circuit concepts, according to the company. The ring oscillator often finds use in such tests because it stresses certain material characteristics and thus indicates how the technology may perform in complete chips, IBM says. The team observed circuit speeds 1 million times faster than previous circuits built using multiple nanotubes—but still far slower than existing silicon devices.

▷**IBM Research**, www.research.ibm.com.



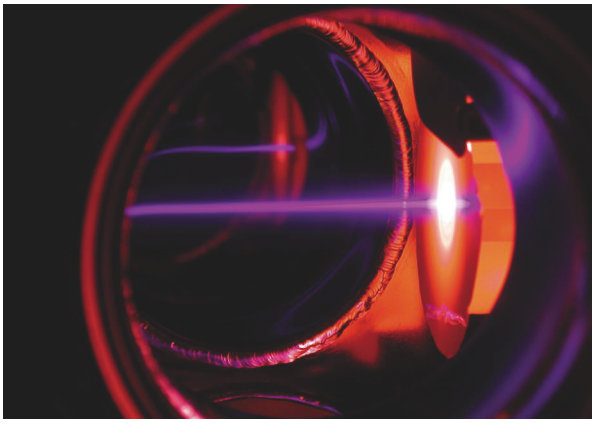
IBM scientists constructed a ring-oscillator circuit around a single carbon nanotube; the 2-nm-diameter nanotube is visible in the inset (right).

Laser-wielding scientists corral wild erbium atoms

Researchers at the NIST (National Institute of Standards and Technology) have used lasers to trap and cool atoms of erbium, a rare earth metal whose unusual magnetic, electronic, and optical properties may be useful in telecommunications, semiconductor manufacturing, and quantum computing. Due to its complex energy structure, erbium has previously proved difficult to contain; its 110 possible energy levels have stymied attempts at laser cooling, which requires precise, controlled manipulation of the atoms' energy emissions.

Magnetic fields and six counter-propagating purple lasers allowed the NIST team to trap more than 1 million atoms in a 100-micron space. Thus incarcerated, the atoms will now yield to further study, and scientists may eventually put them to work emitting photons for telecom applications or doping semiconductor materials.

▷**National Institute of Standards and Technology**, www.nist.gov.



NIST scientists used six purple lasers to cool and trap atoms of erbium, an elusive metal with potentially useful properties.

Enslaved viruses build tiny batteries

05.25.06

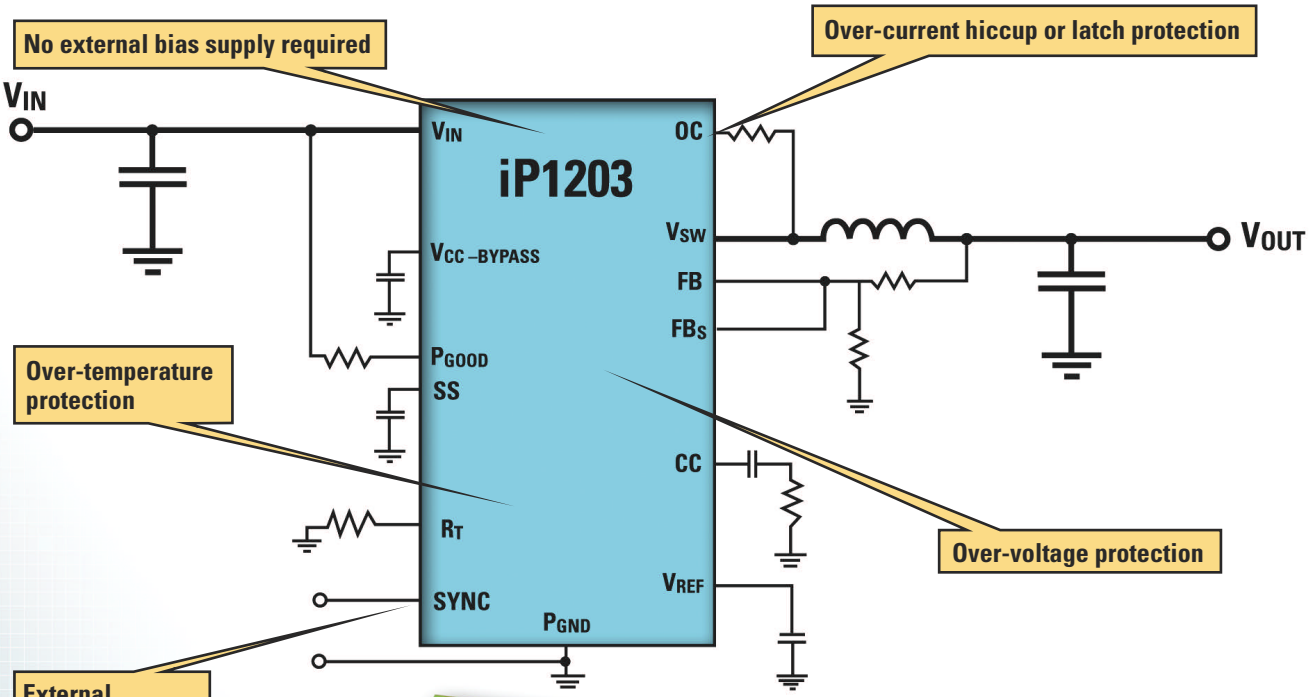
Scientists at the Massachusetts Institute of Technology have altered the genes of a common virus to self-assemble into the anode of a yet-to-be-built lithium-ion battery. Genetic manipulation causes the microbes to make proteins on their coats that collect molecules of cobalt-oxide and gold in a room-temperature reaction. When scientists coaxed these metal-plated viruses to align on a polymer sheet, the viruses formed wires 880 nm long and 6 nm in diameter.

The MIT researchers state that, once these virus-based anodes become parts of complete manufactured batteries, the anodes will deliver energy density two to three times better than existing materials, thanks to their nanoscale structure. The group aims to build batteries ranging from the size of a rice grain to the size of current hearing-aid batteries.

▶**Massachusetts Institute of Technology**, www.mit.edu.

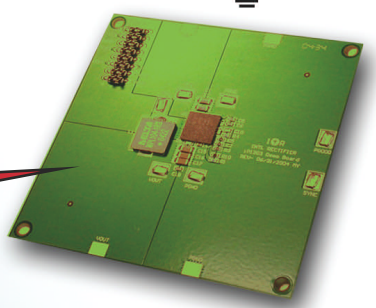
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Reference Designs Available

IRDCiP1201-A
IRDCiP1202-A
IRDCiP1203-A



Part #	Package	V_{IN} (min/max)	V_{OUT}	I_{OUT}	Frequency
iP1201	BGA 9.25mm x 15.5mm x 2.6mm	3.14V to 5.5V	0.8V-2.5V for 3.3V_{IN} 0.8V-3.3V for 5V_{IN}	15A dual 30A single	200 - 400kHz
iP1202	BGA 9.25mm x 15.5mm x 2.6mm	5.5V to 13.2V	0.8V-5V for 12V_{IN} 0.8V-3.3V for <6V_{IN}	15A dual 30A single	200 - 400kHz
NEW iP1203	LGA 9mm x 9mm x 2.3mm	5.5V to 13.2V	0.8V-8.0V for 12V_{IN} 0.8V-3.3V for <6V_{IN}	15A single	200 - 400kHz

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BY HOWARD JOHNSON, PhD

Hidden schematic

I've invited my good friend, Bruce Archambeault, PhD, creator of the IBM EMC-rule-checking program "EMSAT," to share his thoughts about ground.

Your schematic is lying. It shows only the intended flow of signal power. It masks details crucial to the operation of unintentional signal pathways, such as crosstalk and EMI. To understand these factors, you must uncover the hidden schematic operating behind your logic diagram. The hidden schematic represents, among other things, the flow of physical current in your pc board. Current never flows "one way," as logic diagrams show; it always makes a loop out to the load and returning to the source. For EMI purposes, the returning current path is as important as the intended signal path. As long as you keep the outgoing and returning signal paths closely aligned, the radiation patterns from the two currents cancel. Interruptions to the returning current path have serious negative effects on the EMI/EMC performance of a pc board. Even slight deviations in the returning current path can dramatically increase emissions.

Logic diagrams completely omit the returning signal path. They presuppose a perfect common reference node—ground—for all signals. This idealized node maintains the same voltage at all points of use.

Anybody can make a good ground system at audio frequencies. But no one can make one at 100 MHz, spread out over the area of a typical pc board.

When the size of your pc board exceeds the signal wavelengths, your solid-plane layers operate in distributed fashion. Perturbations slosh across the plane from side to side. The instantaneous voltages at different parts of the plane differ markedly, rendering meaningless the concept of a universal common ground reference.

Ground is a good place to grow potatoes and carrots.

When my students ask me how to use ground, I say, "Ground is a good place to grow potatoes and carrots."

I focus my attention not on ground, but on the physical relation of each signal trace to its nearest local-reference plane. That nearest plane, regardless of the dc voltage it carries, forms the main conduit for high-frequency returning signal current.

For example, consider a trace routed next to a power layer. The EMI performance of that trace hinges on the continuity of the power layer. If the trace crosses a chopped-up power region, the boundary of that region interrupts the path of returning signal current on the power layer. In a related way, changing layers within the pc board interrupts the flow of returning signal current.

Remember: Signal current always returns to its source. If you interrupt the natural path of the returning signal current, it will find another way home. The only question is whether the returning signal current remains close to the outbound signal current on a smooth, continuous solid plane or takes a stray path elsewhere that causes EMI problems.

Today's high-speed, complex pc boards have many layers. Who has time to examine each critical signal for a good returning-current path?

I don't, but my computer does. It uses automated EMC-rule-checking tools. These tools uncover the hidden schematic, examining each net in turn, regardless of the pc-board complexity.

If you have not investigated this new class of tool, it's time to do so. Look for a tool that interfaces well with your design process, is easy-to-use, and can display rule violations in a graphical and easy-to-understand manner. EDN

MORE AT EDN.COM

Go to www.edn.com/060525hj and click on Feedback Loop to post a comment on this column.

Howard Johnson will be back in an upcoming issue. You can reach Bruce Archambeault through www.mossbayeda.com, and you can reach Howard Johnson at www.sigcon.com and howie03@sigcon.com. Comments invited!



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Wide V_{IN} Step Down Controller **page 6**

Multi-Function Power Supervisor Saves Cost and Board Space **page 7**

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Amplify Your Performance with Advanced Signal Processing

World's Fastest Triple Video ADC..... **page 2**

8MHz Rail-to-Rail Composite Video Driver in 6 Ld Chipscale Package..... **page 3**

Dual-Protocol Interface Transceivers with 15kV ESD Protection **page 4**

Light-to-Digital Converter in 3mm x 3mm ODFN package **page 5**

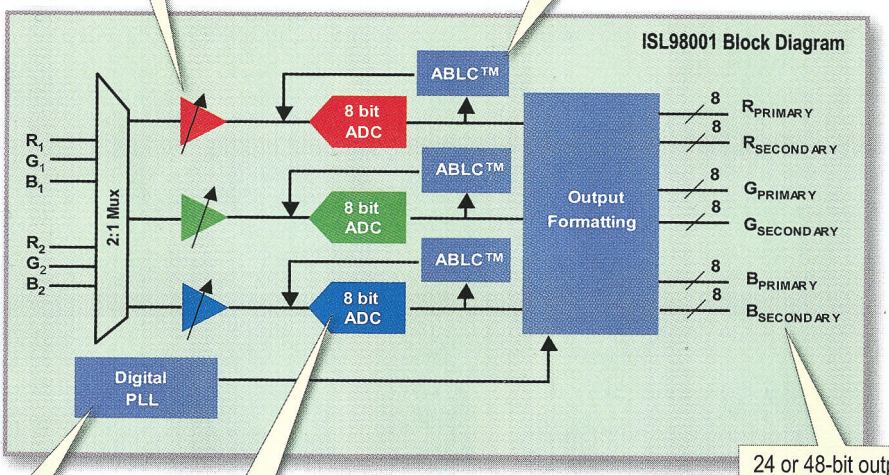
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SPEED GRADE	MAC PC MODE	MAX VIDEO MODE
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ISL98001-170	UXGA 60Hz	1080p
ISL98001-210	WUXGA 60Hz	1080p
ISL98001-240	UXGA 85Hz	1080p
ISL98001-275	QXGA 60Hz	1080p

Key Features

- 140MSPS, 170MSPS, 210MSPS, 240MSPS and 275MSPS maximum conversion rates
- Extremely fast recovery from VCR head switching
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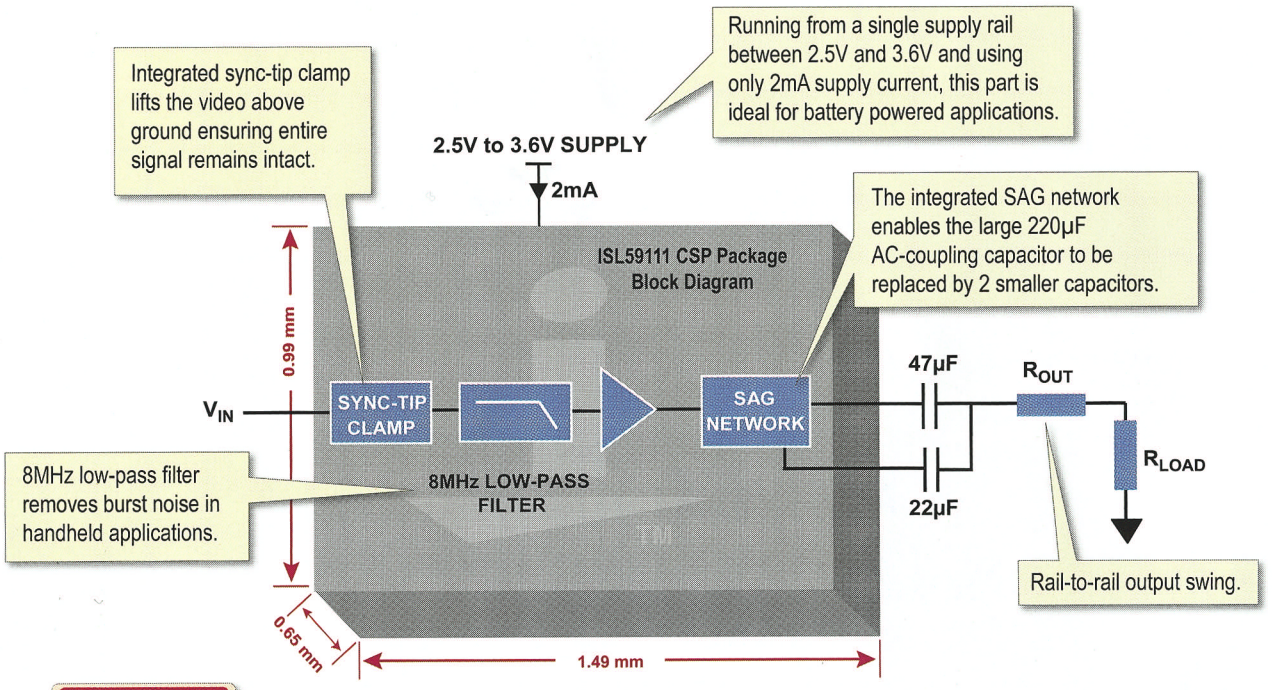
Key Specifications

Device	Resolution (bits)	Max Conversion Rate (MSPS)	Typical PLL Jitter (ps) (p-p)	Sample Phase Choices	Programmable Input Bandwidth (MHz)	CSYNC and SOG Support	Typical Power Dissipation @ Max Conversion Range (mW)	Package
ISL98001-140	8	140	250	64	100 to 780	X	950	128 Ld MQFP
ISL98001-170	8	170	250	64	100 to 780	X	1050	128 Ld MQFP
ISL98001-210	8	210	250	64	100 to 780	X	1100	128 Ld MQFP
ISL98001-240	8	240	250	64	100 to 780	X	1150	128 Ld MQFP
ISL98001-275	8	275	250	64	100 to 780	X	1200	128 Ld MQFP

Rail-to-Rail Amplification in the Tiniest of Packages

Available in Pb-Free Package

Minimal supply current requirements for battery-operated video met in a 1.5mm^2, 8MHz rail-to-rail composite driver.

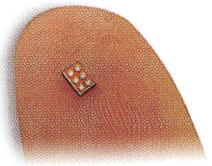


Key Features

- Shutdown current <2µA
- Minimal 2mA supply current reduces battery drain
- 2.5V to 3.6V supply rails
- 3-pole filter has -3dB roll-off at 8MHz
- Input signal DC restroration using a sync-tip clamp
- Faster power-down in 14ns
- Output current of 40mA to drive composite video
- Tiny, low-profile chipscale package. ISL59110 and ISL59112 available in SC-70 package.



6 Ld CSP



Key Specifications

Device	# of Amps	Slew Rate (V/µs)	V_S (min) (V)	V_S (max) (V)	V_N (nV/√Hz)	BW @ -3dB (MHz)	Rail-to-Rail	Gain A_V (min) (V)	I_S (per amp) (mA)	I_{BIAS} (µA)	I_{OUT} (mA)	V_{OUT} (V)	Diff Gain (%)	Diff Phase (°)	V_{OS} (max) (mV)	A_{VOL} or A_{ZOL} (dB or V/mA)	Package
ISL59110	1	70	2.5	3.6	N/A	8	YES	2	2	5	40	3.2	0.1	0.05	N/A	N/A	6 Ld SC-70 T+R
ISL59111	1	70	2.5	3.6	N/A	8	YES	2	2	5	40	3.2	0.1	0.005	N/A	N/A	6 Ld CSP
ISL59112	1	85	2.5	3.6		40	YES	2 (fixed)	2	5	40	3.2	0.02	0.04	N/A	N/A	6 Ld SC-70 T+R

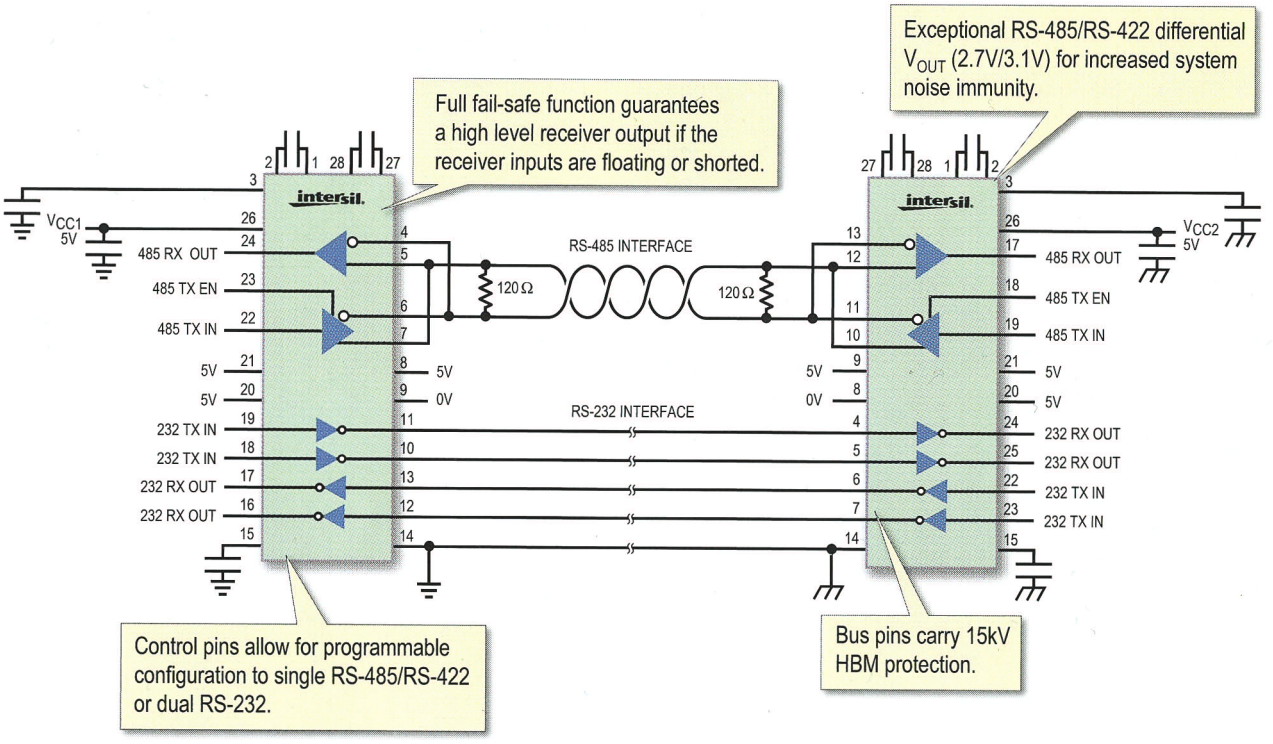
Smaller-Sized, Superior Protection in Dual-Protocol Transceivers from Intersil

Best-in-class components offering 15kV ESD protection in a space-saving QFN package option.

Available in Pb-Free Package



40 Ld QFN is 75% smaller than standard SOIC



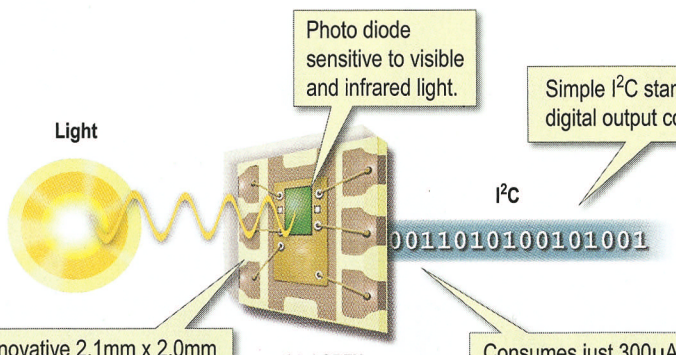
Key Specifications

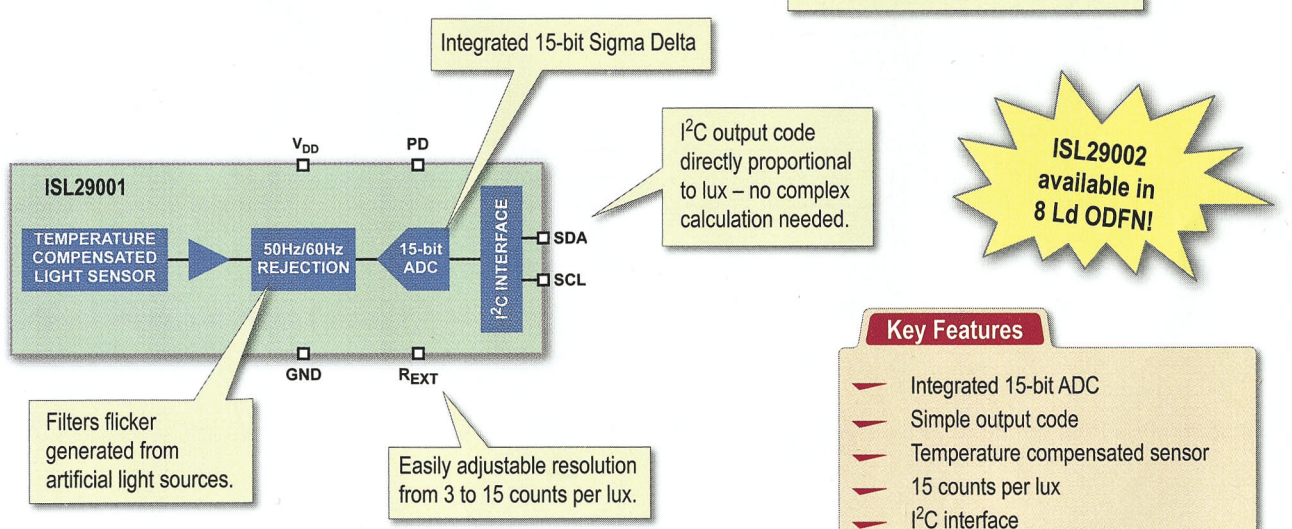
Device	Supported Protocols	# of Ports	# of Tx/Rx per Port	High ESD (kV)	Data Rate RS-485/RS-232 (Mbps)	RS-485 Rx Fail-safe Type	V_{LOGIC} Supply Pin?	RXEN Polarity	Loop-back Feature?	Operating I_{CC} RS-485/RS-232 (mA)	SHDN I_{CC} (µA)	V_{CC} (V)	Package
ISL81387	RS-232, RS-422, RS-485	1	1/1 RS-485, RS-422; 2/2 RS-232	15	20, 0.46/0.5	Full	No	High	Yes	1.6/3.7	30	5	20 Ld SOIC, 20 Ld SSOP
ISL41387	RS-232, RS-422, RS-485	1	1/1 RS-485, RS-422; 2/2 RS-232	15	20, 0.46, 0.115/0.5	Full	Yes	High and Low	Yes	1.6/3.7	30	5	40 Ld QFN
ISL81334	RS-232, RS-422, RS-485	2	1/1 RS-485, RS-422; 2/2 RS-232	15	20/0.5	Full	No	None	Yes	1.6/3.7	42	5	28 Ld SOIC, 28 Ld SSOP
ISL41334	RS-232, RS-422, RS-485	2	1/1 RS-485, RS-422; 2/2 RS-232	15	20, 0.46, 0.115/0.5	Full	Yes	Low	Yes	1.6/3.7	80	5	40 Ld QFN

Intersil's New Light-to-Digital Converters Provide Pure 15-bit I²C Digital Data

Patterned upon the human eye, these integrated light sensors generate 15-bit effective resolution.

Available in Pb-Free Package





Key Features

- Integrated 15-bit ADC
- Simple output code
- Temperature compensated sensor
- 15 counts per lux
- I²C interface
- 2.5V to 3.3V supply
- -40°C to +85°C temperature range

Key Specifications

Device	Peak Spectral Sensitivity (nm)	Supply Voltage (min) (V)	Supply Voltage (max) (V)	Supply Current (µA)	Lux Range (max) (Lux)	Counts per Lux (max) (Counts/ Lux)	Output Interface	Output Resolution (bits)	Integration Time (ms)	Package Dimensions (mm)	Pb-Free?	Enable Pin?	Package
ISL29001	550	2.25	3.63	280	10,000	15	I²C	15	100	2x2.1x0.7	Y	Y	6 Ld ODFN
ISL29002	550	2.25	3.63	400	50,000	15	I²C	15	100	3x3x0.7	Y	Software Enabled	8 Ld ODFN

4.5V to 28V Wide V_{IN} and Adjustable Operating Frequency Offers Design Flexibility and Ease in General Purpose Applications

ISL6420A wide V_{IN} Step Down controller combines control, output adjustment, monitoring and device protection in a single component.

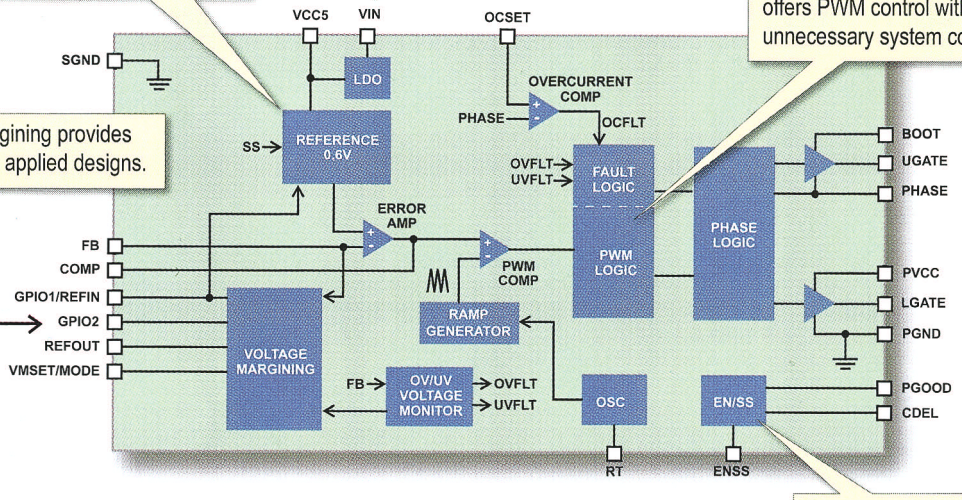
Available in Pb-Free Package

Excellent output voltage regulation (0.6V internal reference; ±1.0% RAOLT) provides unmatched stability throughout.

Broad voltage input range (4.5V to 28V) offers flexibility and use in a variety of applications.

Simple single-loop control design offers PWM control without unnecessary system complexity.

Output voltage margining provides added safety to the applied designs.



Programmable soft-start available through EN/SS pin capacitor value setting.

Key Features

- Operates on a 4.5V to 28V input range
- Diode emulation during start-up for pre-biased load applications
- Adjustable operating frequency from 100kHz to 1.4MHz offering potential cost and space savings
- Programmable soft-start available through EN/SS pin capacitor value setting
- Voltage margining protects your design

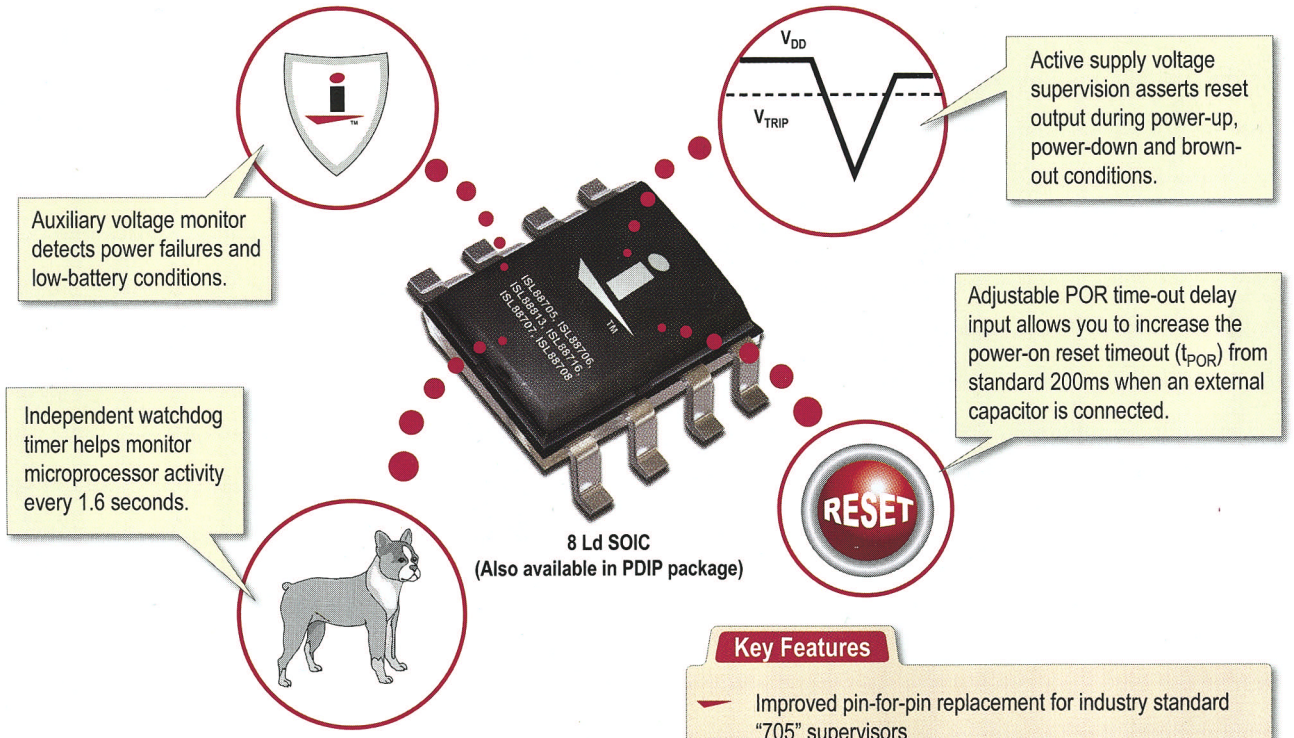
Key Specifications

Device	Device Description	V_{IN} (min) (V)	V_{IN} (max) (V)	V_{OUT} (min) (V)	V_{OUT} (max) (V)	I_{OUT} (max) (A)	V_{BIAS} (V)	I_{CC} (min) (mA)	I_{CC} (typ) (mA)	Package
ISL6420A	PWM Controller with Wide V_{IN}, Start-Up into Pre-Bias Load	4.5	28	0.6	V_{IN}-0.5V	20	5	1.4	2	20 Ld QFN, 20 Ld QSOP
ISL6420	Advanced Single Synchronous Buck Pulse-Width Modulation (PWM) Controller	4.5	16	0.6	V_{IN}-0.5V	20	5	1.4	2	20 Ld QFN, 20 Ld QSOP

Multi-Function Integration Excellence in a Power Supervisor Saves Cost and Frees Board Space

Protect your system and improve reliability with the ISL887XX/813 family.

Available in Pb-Free Package



Key Features

- Improved pin-for-pin replacement for industry standard "705" supervisors
- Ultra-low 10µA supply current
- ±1.8% voltage trip point accuracy
- Added time-out adjustability on POR is an industry first for voltage supervisors

Key Specifications

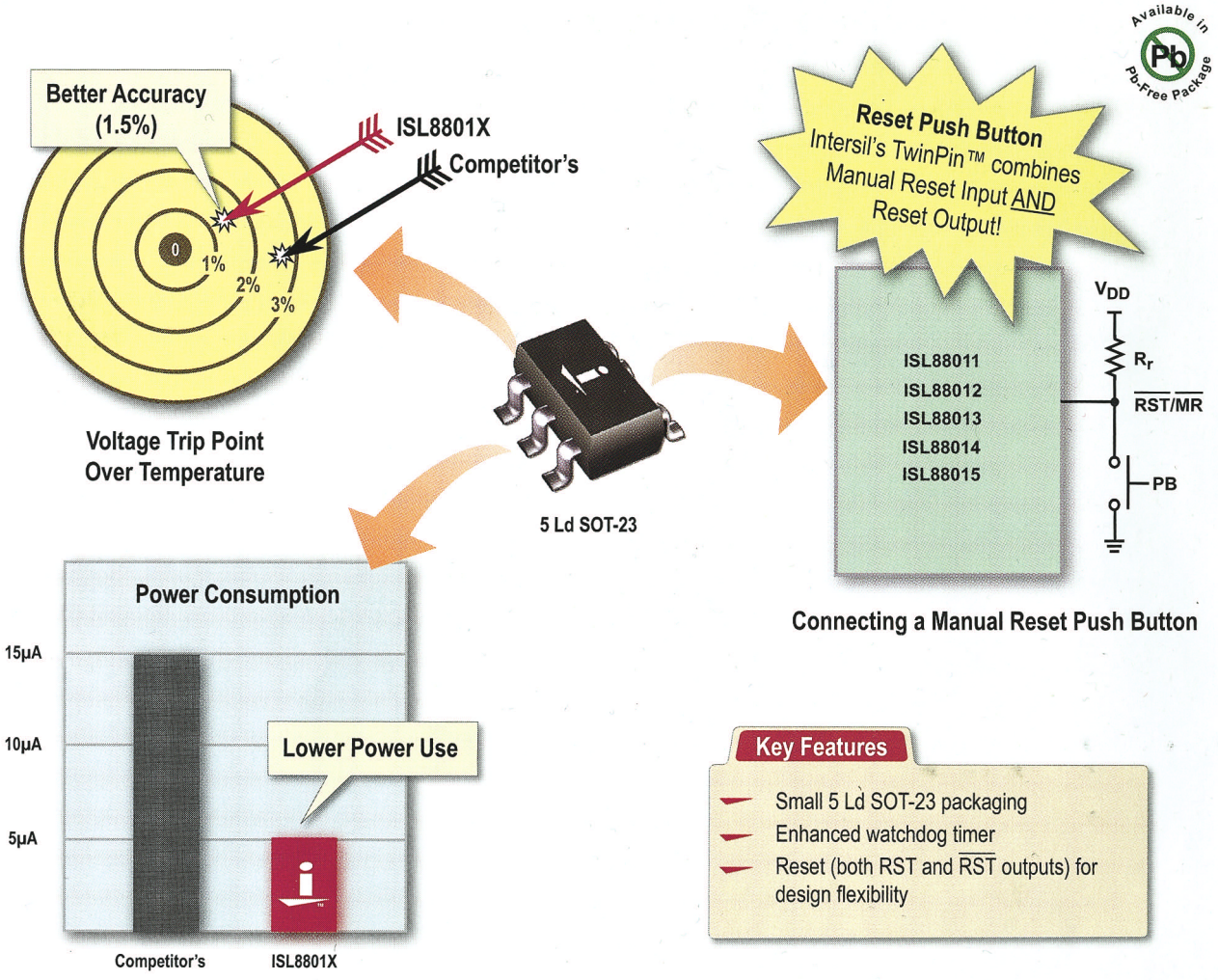
Device	Number of Voltage Monitors	Fixed V_{TRIP}	Adj. V_{TRIP} (Resistors)	Open-Drain $\overline{RST}$	Push-Pull RST	Manual Reset	WDI/WDO	Adj. POR Timeout	Package
ISL88705	2	Y	Y	Y		Y	Y		8 Ld PDIP, 8 Ld SOIC
ISL88706	2	Y	Y	Y		Y	Y		8 Ld PDIP, 8 Ld SOIC
ISL88707	2	Y	Y	Y	Y	Y		Y	8 Ld PDIP, 8 Ld SOIC
ISL88708	2	Y	Y	Y	Y	Y		Y	8 Ld PDIP, 8 Ld SOIC
ISL88813	2	Y	Y		Y	Y	Y		8 Ld PDIP, 8 Ld SOIC
ISL88716	2	Y	Y		Y	Y	Y		8 Ld PDIP, 8 Ld SOIC

Intersil Voltage Supervisors

High Performance Analog

Get High-Precision Accuracy with Low Power Consumption

The ISL8801X family provides improved voltage monitoring accuracy with low power and a host of other key features.



Key Features

- Small 5 Ld SOT-23 packaging
- Enhanced watchdog timer
- Reset (both RST and $\overline{RST}$ outputs) for design flexibility

Key Specifications

Device	Number of Voltage Monitors	Fixed V_{TRIP}	Adj. V_{TRIP} (Resistors)	Open-Drain RST	Push-Pull RST	Push-Pull RST	TwinPin™ MR/RST	Enhanced WDT	Adj. POR Timeout	Package
ISL88011	1	Y		Y	Y	Y	Y		Y	5 Ld SOT-23
ISL88012	2	Y	Y	Y	Y	Y	Y			5 Ld SOT-23
ISL88013	1	Y		Y	Y	Y	Y	Y		5 Ld SOT-23
ISL88014	1		Y	Y			Y		Y	5 Ld SOT-23
ISL88015	1		Y	Y			Y	Y		5 Ld SOT-23

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- ☑ Signal-to-noise ratio >80dB
- ☑ VA supply receive current 350µA typical
- ☑ Amplifier transit current 1Ap-p into 0.9Ω
- ☑ On-board application CPU
- ☑ SPI host interface
- ☑ RoHS-compliant 38TSSOP and 64LQFP IC packages
- ☑ Operating temperature -40 to +85°C
- ☑ DSK with Gerber files
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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Scaling: a balanced view, part two

In the last installment of Analog Domain, I began a summary of Klaas Bult's analysis on the effect of technology scaling on power dissipation (**references 1** and **2**). This column replicates the minimum-circuit model and Bult's Algorithm for reference (**figures 1** and **2**). The algorithm depends on three process-dependent quantities and eight application-dependent parameters. It calculates six circuit measures, the last of which is the minimum power dissipation for the minimum circuit. Bult's analysis does hang on a few assumptions, but more than a decade of silicon-process history supports them, as do the foreseeable trends in silicon-process development.

The first value to calculate is the maximum V_{DD}. Ignoring the slight rise in the apparent dielectric strength of ultrathin films compared with thicker film and bulk samples, V_{DD} is essentially proportional to gate-oxide thickness, T_{OX}. T_{OX}, in turn, scales directly with the process's minimum feature size, L_{MIN}, by a ratio that has held essentially constant over process evolutions that saw L_{MIN} decline from 3 microns to 60 nm:

$$\lambda = \frac{T_{OX}}{L_{MIN}} \approx 0.03.$$

Linear circuits require head room between the signal swing and the supply rails. Bult's model captures this quantity in the form of a *voltage efficiency*, η_{VOL}:

$$\eta_{VOL} = \frac{V_{SIG(-P)}}{V_{DD}}.$$

Setting η_{VOL} to a reasonable constant value, say 80%, gives the maximum peak-to-peak signal amplitude, V_{SIG}.

The application determines the necessary dynamic range:

$$DR = \frac{V_{SIG(RMS)}}{\sqrt{\sum_i V^2_{UNWANTED}(i)}};$$

$$V_{SIG(RMS)} = \frac{V_{SIG(P-P)}}{2\sqrt{2}},$$

where $V_{UNWANTED}$ refers to the various voltage-error terms, including white noise, 1/f noise, and offset.

Though $V_{UNWANTED}$ results from the combination of multiple sources, often in practice one term dominates. As a result, the load-capacitance calculation depends on which term is most important to the application.

Applications that are sensitive to offset voltage require a high degree of device matching. Below the 700-nm node, the minimum capacitance to attain a given degree of matching varies in proportion to $1/L_{MIN}$. (Calculations are available in **Reference 2**.) The minimum capacitance for a given dynamic range for circuits in which either white noise or 1/f noise is the dominant consideration varies as $1/L_{MIN}^2$. At the 90-nm node, the minimum capacitance for matching is about 200 times larger than the minimum capacitance for white noise, which is about 200 times larger than the minimum capacitance for 1/f noise. For this reason, circuits that demand a high degree of dc accuracy often use device averaging and offset-cancellation techniques.

Given the minimum capacitance that the circuit requires to attain the specified dynamic range, you can calculate the drive current necessary to meet bandwidth, slew-rate, settling-time, and distortion criteria. The next installment of this column will pick up from here. EDN

REFERENCES

1 Israelsohn, Joshua, "Scaling: a balanced view, part one," *EDN*, March 30, 2006, pg 40, www.edn.com/article/CA6317072.

2 Bult, Klaas, "The effect of technology scaling on power dissipation in analog circuits," International Solid-State Circuits Conference 2006, Feb 5, 2006.

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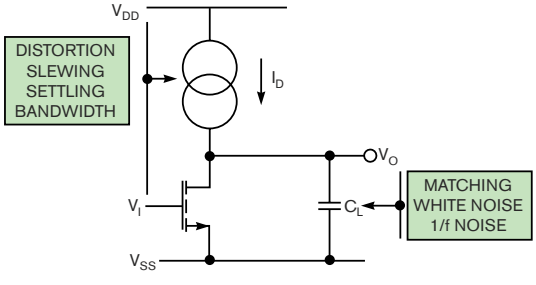


Figure 1 A single-transistor gain stage serves as Bult's model minimum subcircuit.

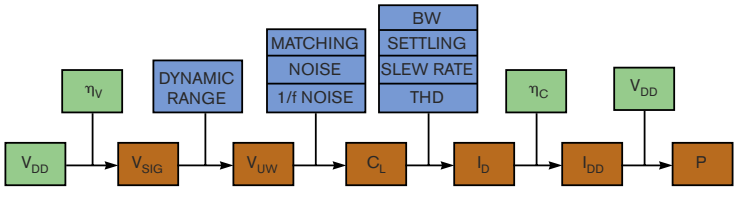
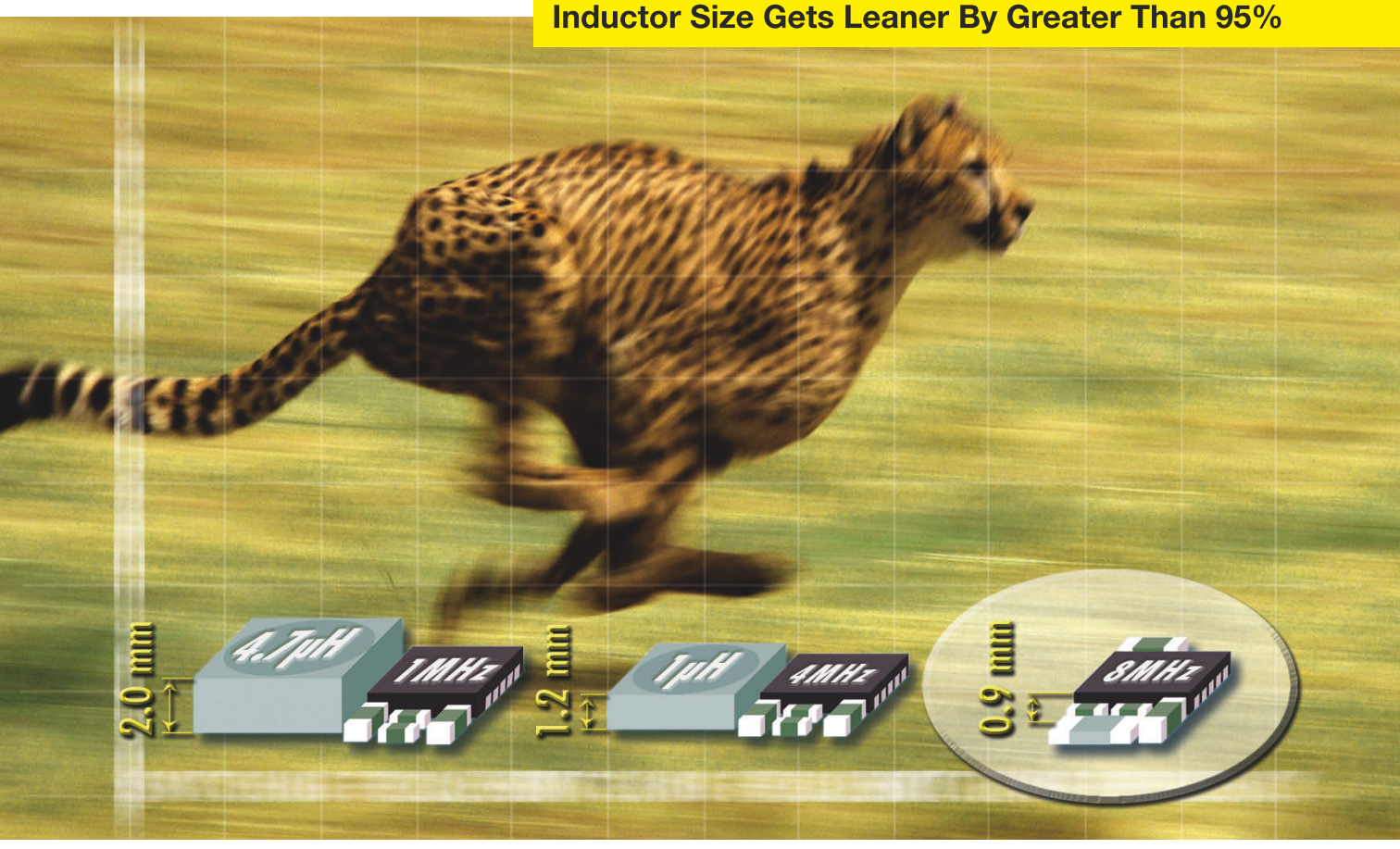


Figure 2 Bult's analysis combines application requirements (blue) with terms that derive from the process scale (green) to generate calculated values (brown) resulting in a power estimate for the model subcircuit.

8MHz

Industry's First 500mA Synchronous Buck Regulator

Inductor Size Gets Leaner By Greater Than 95%



Micrel's MIC2285 is a high efficiency 8MHz pulse width modulated (PWM) synchronous buck (stepdown) regulator. It features a LOWQ™ LDO standby mode that draws only 20µA of quiescent current. The MIC2285 is the industry's breakthrough ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the MIC2285 operates with a constant frequency 8MHz PWM control. Under light load conditions, such as those in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load LOWQ mode, the LDO maintains the output voltage and draws only 20µA of quiescent current. The LDO mode of operation saves battery life and does not introduce spurious noise and high ripple which is common place in pulse skipping or bursting mode regulators. The MIC2285 operates from a 2.7V to 5.5V input voltage and features internal power MOSFETs that can supply up to 500mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low-dropout conditions.

For more information, contact your local Micrel sales representative or visit us at: www.micrel.com/ad/mic2285.
Literature: 1 (408) 435-2452 Information: 1 (408) 944-0800

The Good Stuff:

- 2.7 to 5.5V supply/input voltage
- Light load LOWQ LDO mode
- 20µA quiescent current
- > 90% efficiency
- Low noise, 75µVrms
- 100% maximum duty cycle
- Adjustable output voltage option down to 1V
- Ultra-fast transient response
- Ultra-small 0.47µH inductor
- Fully integrated MOSFET switches
- Micropower shutdown operation
- Thermal shutdown and current limit protection
- Pb-free 10-pin 3mm x 3mm MLF™ package
- –40°C to +125°C junction temperature range

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Reference designs matter, as this TV design illustrates

You might wonder why we would choose a TV design as a milestone in our 50th-anniversary review of key events that had lasting impact. Well, the TV clearly had a lasting impact, and, at the time, using transistors in TVs was leading-edge technology. But this Texas Instruments (www.ti.com) design probably isn't milestone-worthy per se. In fact, TI clearly stated that it had no intention of manufacturing the TV set. Instead, the TI engineers set out to prove the viability of using transistors in a TV design, hoping that their work would lead TV manufacturers to adopt transistors in place of vacuum tubes. You can go to www.edn.com/060525mtm to read the entire story and see a schematic; the **sidebar** "Self-contained TV receiver uses 24 transistors" is an excerpt. Nowhere in the original article will you find the term "reference design," but that's precisely what TI's engineers created. Today, the reference design is more important than ever.

Take, for example, a mobile handset, a DVD recorder, or even a subsystem, such as the optical pickup unit in a DVD player/recorder. The reference design is paramount. For the product-design team, the reference design jumpstarts the project and allows the team to meet shrinking market windows. For the vendor of the chip at the center of the design, the quality of that vendor's reference design may be more important than the chip itself in winning business. And, for vendors of support chips and components, getting a reference design to include one of their components can be more important that calling on the end customer.

In *EDN*'s first Global Report in November 2004, we covered the importance of reference designs in "Adaptive engineering" (www.edn.com/article/CA474470). Product managers from LSI Logic (www.lsilogic.com) recounted how some manufacturing houses would use an unchanged version of the company's DVD-recorder reference design, which it based on an ASSP (application-specific standard product). That use would also include the provided user interface and software based on Wind River Systems' (www.windriver.com) VxWorks. Other manufacturers with more available engineering resources would optimize the design with custom software, attempting to differentiate their products. But in both cases or anywhere in between, the reference design was a key to winning business.

The maker of a DVD player buys laser drivers only in the form of optical-pickup-unit subsystems.

Perhaps the account of National Semiconductor's (www.national.com) selling laser drivers for DVD players and recorders was even more telling. The maker of a DVD player buys laser drivers only in the form of optical-pickup-unit subsystems. In such a case, the component vendor may need to win a spot in a reference design or a spot in the actual subsystem design to sell the product.

Reference designs drive our industry in everything from power-management subsystems in MP3 players to complete designs of products, such as Bluetooth-based hands-free kits for mobile handsets. Reference designs are milestone-worthy. EDN

09.01.58

FROM THE VAULT

Self-contained TV receiver uses 24 transistors

Twenty-four transistors and one high-voltage rectifier tube perform all of the functions required to develop a high-definition picture and accompanying sound in a completely self-contained portable television receiver. Power is furnished by a 10-cell nickel-cadmium battery providing 12V at 700 mA, average current. The picture tube employed in this receiver is a 9QP4 whose filament has been modified to operate at 12V with 150 mA.

Two tuners were developed for this receiver. The more sensitive one uses tetrode transistors in the RF amplifier, mixer and oscillator. Its disadvantages lie in a much higher cost and a 12- to 14-dB noise figure. The second tuner uses two 2N623 diffused-base transistors in the mixer and oscillator stages, with no RF amplifier. Noise figure is 9 to 11 dB, but overall tuner gain is only 10 to 12 dB on channel 13. This compares with an overall tuner gain of 20 to 22 dB (channel 13) for the tetrode tuner. Cost is considerably lower for this unit and is said to compare favorably with current vacuum-tube tuners.

This receiver was developed by Roger Webster and Harry Cooke of the Circuit Development branch of Texas Instruments Inc (Dallas). The purpose of this work was to determine the feasibility of designing a transistorized television receiver using Texas Instrument units. There is no intent by this firm to manufacture such receivers.

—*EDN*, September 1958

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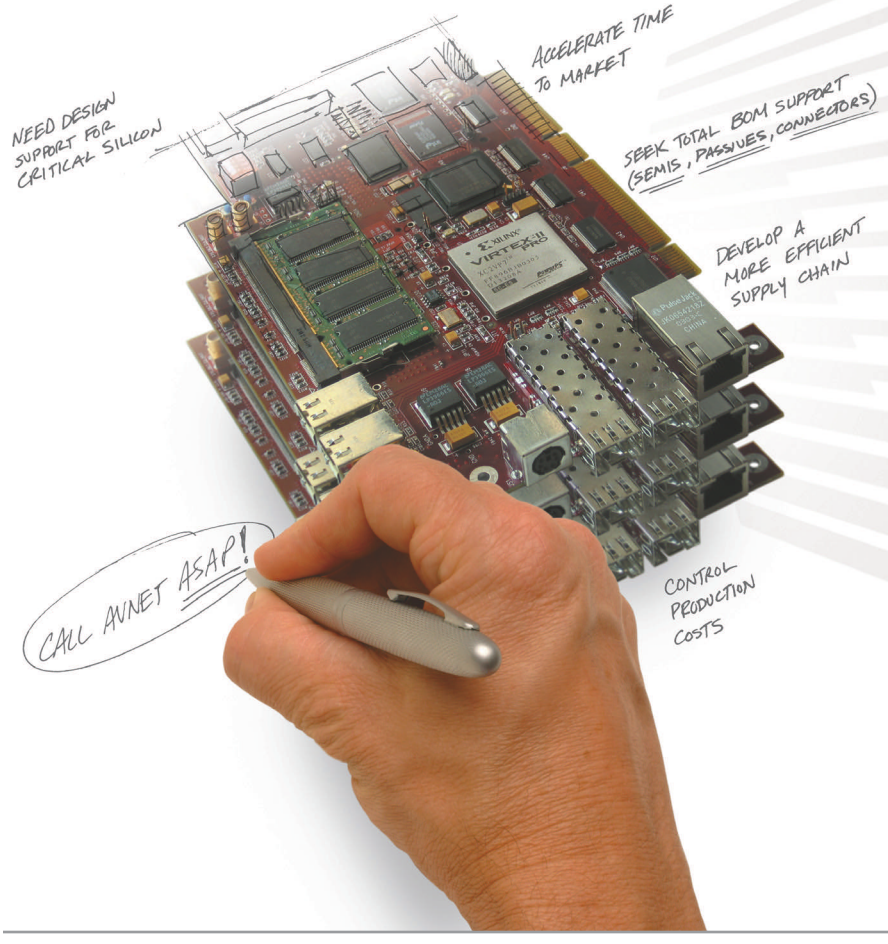
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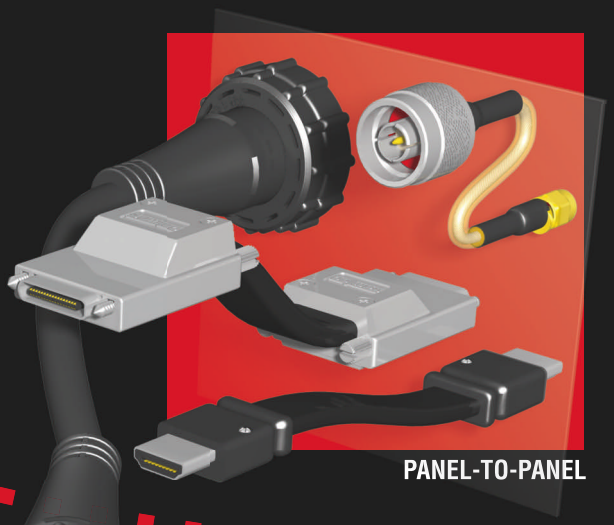
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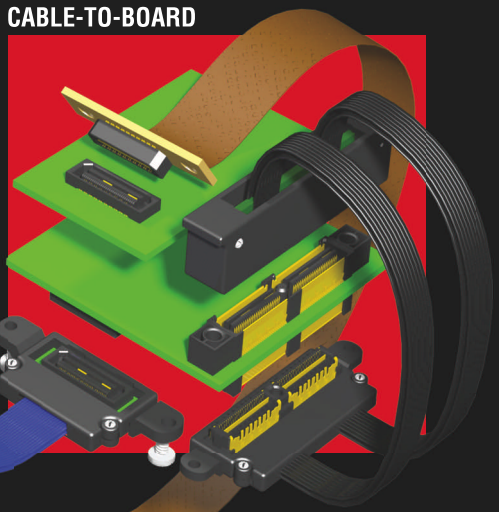


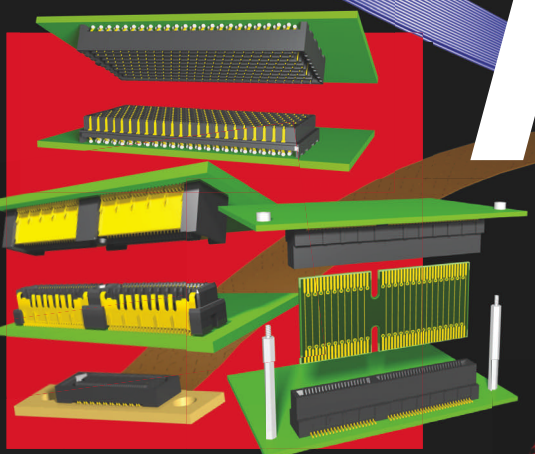
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PANEL-TO-BOARD



CABLE-TO-BOARD





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BY WARREN WEBB • TECHNICAL EDITOR

DISPLAYS INVADE EMBEDDED-SYSTEM SPACE



FULL-COLOR GRAPHICS DISPLAYS IN HIGH-VOLUME CONSUMER PRODUCTS, SUCH AS MOBILE PHONES AND MUSIC PLAYERS, HAVE CAPTURED THE ATTENTION OF THE PUBLIC AND SET NEW STANDARDS FOR EMBEDDED-DEVICE DESIGN.

Figure 1 Electronic-paper displays from E Ink contain millions of bistable microcapsules that change color with an activating charge.

As prices plummet, embedded-system designers are turning to graphical displays to simplify operation, ease system upgrades, and distinguish their products. Designers of traditional embedded products focused on maximizing performance with less emphasis on the user interface. However, the dazzling full-color graphics in today's PCs, mobile phones, and other portable consumer devices have raised consumer expectations for all electronic products. These rising user-interface expectations, along with ubiquitous networking, have redefined traditional embedded-design rules. Newer embedded products are not necessarily limited in computing and memory resources and may easily require more processing power for communications and a graphical display than for the application.

A graphical-display system allows a designer to create a simple operator interface that sequentially deals with a single command or function at a time. The designer can "hide" most of the complexity and auxiliary features until they are necessary to simplify operation. A graphical-display interface is your product's first impression and provides an obvious way to differentiate your product from your competitors' products. Designers can use graphics to create a unique look and feel for their products and deliver a similar theme across an entire product line. When you couple a graphics display with a touchpanel overlay, the user can simulate almost any front-panel configuration and still be able to add or change features with a firmware modification.

A display system may be able to ease product-development-schedule problems and offer additional or recurring revenues. Prod-

AT A GLANCE

- The recent popularity of consumer devices with full graphics displays puts pressure on embedded-system designers to match the user experience.
- Although internally complex, a graphical display simplifies the user interface by hiding auxiliary functions and features until the user needs them.
- A well-designed embedded device with a graphical user interface may survive product changes and updates without hardware modifications.
- Several vendors offer complete drop-in graphics subsystems that act as stand-alone serial peripherals to embedded processors.
- Embedded-system developers can replace user-interface hardware with a communications link to common external consumer devices.

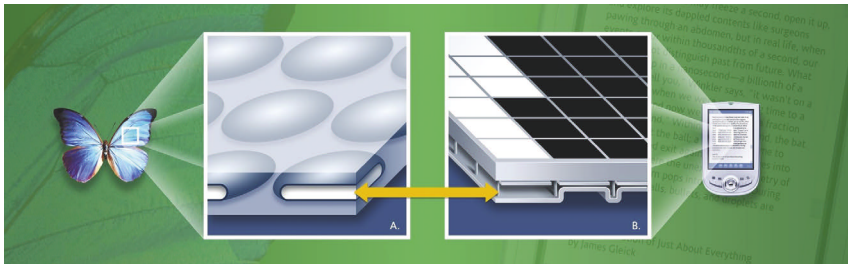


Figure 2 Qualcomm's IMOD technology combines MEMS structures with thin-film optics to duplicate the light interference iridescence in nature.

uct design is always a compromise between first to market and the best set of features. A flexible graphics interface, along with a built-in network connection, offers the option of shipping the product with an initial set of features and then upgrading firmware over the network to meet competitive pressures or to fix problems. Another marketing strategy is to offer a limited-function device at a low price and then offer to sell the user optional, remotely activated features or services. Either approach requires a well-designed, general-purpose hardware platform with an adaptable graphics unit and sufficient system resources to accommodate future software applications.

DISPLAY PROCESSOR

Designing a display-based interface into an embedded product is a major undertaking with significant impact on cost and scheduling. An application that once required an 8-bit processor may need a second CPU or an upgrade to 16 or 32 bits when you take graphics into consideration. A graphics subsystem also consumes substantial memory and power resources. Combining graphics processing with a legacy embedded-system task may also require the addition of a real-time operating system to maintain timing performance for the application. In addition, the display unit requires a new power source and mechanical packaging.

Designers have several alternatives to integrating a graphics display into an embedded device. The most radical approach is to redesign the device with a new processor section that can support both the embedded task and the graphics display. The software team can then develop a custom graphics library for the embedded-system application. Although this method probably requires extensive NRE (nonrecurring-engineering) costs, it should produce the most efficient system with the least expensive production hardware. A less intrusive approach is to treat the graphics section as an external peripheral with a communications channel to the embedded processor. This technique allows developers to choose off-the-shelf graphics and software elements to minimize development costs.



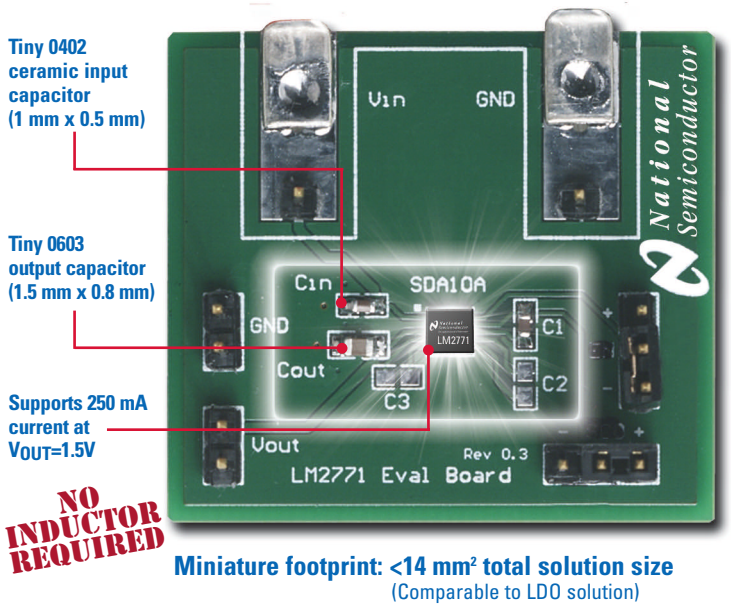
Figure 3 Sharp Microelectronics' 3.5-in., quarter-VGA TFT LCD targets low-power, portable designs requiring high-brightness displays.

Active-matrix-LCD screens are the most popular graphics-output devices for embedded systems because of their low power requirements, low weight, superior image quality, and fast response. LCDs sandwich cells of a light-polarizing liquid between two perpendicularly polarized glass panels that a matrix of TFTs (thin-film transistors) drives. An electric current changes the polarization characteristics of the liquid and blocks light transmission through that cell. Expanding on this basic principle, manufacturers offer a wide array of high-resolution, monochrome and color LCD panels to fit most embedded-system applications. Many designers combine an LCD panel with a resistive touchscreen or several variable-function input switches to form the complete user interface.

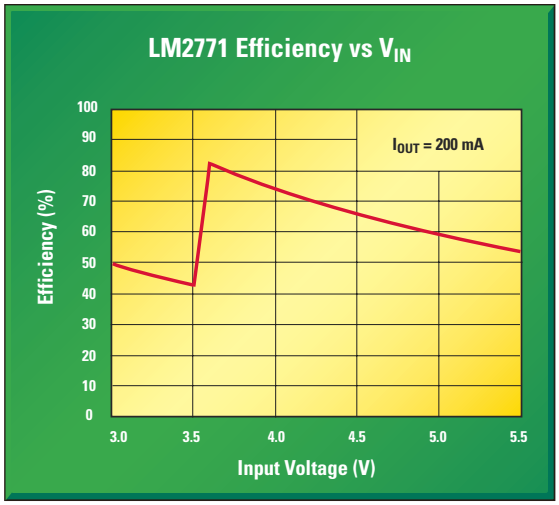
OLED (organic-LED)-display technology, which Eastman Kodak developed more than 20 years ago, are gaining popularity in embedded-system applications because the technology offers potentially brighter, higher contrast images with less power and lower manufacturing costs than LCDs. OLEDs sandwich several organic films between a metallic cathode and a transparent anode. The carbon-based films comprise a hole-injection layer, a hole-transport layer, an emissive layer, and an electron-transport layer. The choice of organic materials and the layer structure determine the color, operating lifetime, and power efficiency. When you apply voltage to the OLED, the injected positive and negative charges recombine in the emissive layer and create electroluminescent light. Unlike LCD panels,

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OLEDs emit light and require no backlighting. OLEDs suffer from reduced yields and limited life span. Further, water can easily damage the matrix.

PAPER DISPLAY

Although the technology has roots in the 1970s, recent advances in manufacturing techniques have renewed interest in electronic-paper displays. These displays possess a paperlike, high-contrast appearance; ultralow power consumption; and a thin, light, sometimes-flexible form (**Figure 1**). It gives the viewer the experience of reading from paper but adds the power of updatable information. Millions of microcapsules, containing a dark fluid and hundreds of tiny, white chips, cover electronic-paper displays. With an activation grid controlling the charge at each microcapsule, you can specify the color at each pixel by forcing the white chips to rise to the surface or sink to the bottom. An advantage of this electronic-ink approach is that the bistable, nonvolatile microcapsules retain their position when you turn off the power. To demonstrate the concept, E Ink offers a Linux-based electronic-paper-development kit that provides an 800×600-pixel display, electronics, and software to construct a battery-powered, portable book reader.

Qualcomm hopes to define the next generation of display technology by combining MEMS (microelectromechanical-system) structures with thin-film optics. The company used as its model the natural microscopic structures on butterfly wings and peacock feathers to produce the IMOD (interferometric-modulator display), which uses interference to modulate the light and create low-power, reflective displays (**Figure 2**). IMOD elements typically measure 10 to 100 microns per side and include a tiny film structure that moves just enough to reflect a precise wavelength of light. The reflective film moves a certain distance, and that distance determines the color of the IMOD elements, each of which represents 400 to 1000 dpi. Designers can group several of these elements to form a single pixel. To create a flat-panel display, Qualcomm fabricates and packages a large array of IMOD elements in the desired format. Finally, the company attaches

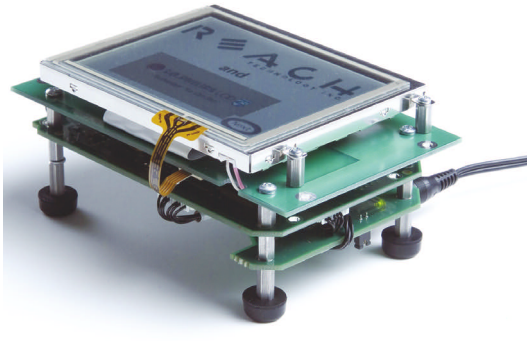


Figure 4 A new, 4-in., color, touch-display module from Reach Technology allows designers to integrate graphics as an intelligent serial device.

driver chips at the elements' edge to complete the display. Because the reflective IMOD requires no backlight, the unit has low power consumption.

Regardless of the technology you select, graphics-software libraries and drivers are essential to any display system. You can obtain control routines from the display manufacturer, third-party vendors, or in-house. Alternatively, the operating system may integrate these routines. Simple drawing libraries include subroutines to render lines, circles, boxes, and a limited selection of text type styles. The next step up is an object-oriented graphics library that includes pushbuttons, sliders, gauges, graphs, and drop-down menus. If you change one or more objects on the screen, library routines automatically redraw the affected objects. The third level of software is the graphics manager, such as Microsoft Windows or X Windows, in which applications can independently control their portions of the display screen. The complexity and software footprint grow depending on the library model you select.

For designers wanting to start with a bare-bones display and develop their own interfaces and custom software, Sharp Microelectronics recently introduced a 3.5-in. transflective TFT-LCD display with 100 cd/m^2 of brightness (**Figure 3**). The quarter-VGA LQ035Q7DH01 module targets portable devices requiring low power consumption and operation in a wide range of lighting conditions. Such applications include GPS (global-posi-



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RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Comparators & Op Amps—May They Never Meet (Or Good Advice From Mr. Punch)

Q. *Why buy an expensive comparator when an op amp is just as good?*



A. Because it isn't. My advice to anyone tempted to use an operational amplifier (op amp) as a comparator is the same as Mr. Punch's advice to those about to marry? "Don't!" But since my good advice is as likely to be taken as Mr. Punch's this piece contains some advice for those who are going ahead anyway.

Comparators have differential inputs and a rail-to-rail output. So do op amps. They have low offset, high gain and high common mode rejection ratio (CMRR). So do op amps. But comparators are designed to work open-loop, drive logic circuits, work at high speed even when over-driven, and accept large differential input voltages. Op amps are intended to work closed-loop, driving simple resistive or reactive loads—and are not designed to recover quickly from overdrive. But op amps are cheaper, often come in four- or even six-packs (so often one is spare and begging to be used), and compared to most comparators, have better offset and bias current specifications.

Using an op amp as a comparator may lead to difficulties for three major reasons: speed, logic drive capability, and various effects of input structures.

Comparators are designed to work with large differential inputs, while op amps are intended for closed-loop operation with both inputs at very similar potentials. If an op amp sees a differential input voltage of even a few millivolts its internal circuitry may saturate. Recovery may be very slow and recovery time may vary considerably with the level of over-drive and from device to device. Such variability and loss of speed may be unwelcome in a comparator.

If an op amp has rail-to-rail output and is operated on the same supplies as the saturating logic it is driving (CMOS or TTL) then interfacing is not hard. But if the op amp and logic supplies differ, then additional interface circuitry, which may be quite complex, is necessary to produce the correct levels.

Finally, op amp inputs usually have high impedance and low bias current. But if a differential input voltage of more than a few hundred millivolts is applied to them this may no longer be the case, and all sorts of less than ideal behaviour may occur. Higher levels of over-drive may also do minor damage to an op amp's input stages, resulting in slowly accumulating long-term changes in performance which may be overlooked during laboratory development.

To learn more about op amps and comparators,
Go to: http://rbi.ims.ca/4922-718



Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

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tioning-system) units, PDAs (personal digital assistants), bar-code scanners, and test equipment. The display features 262,144 colors, power consumption of less than 365 mW, a contrast ratio in transmissive mode of 100-to-1, and an operating temperature of −10 to +70°C. Including the LED-backlight system, the display module measures only 4 mm thick and weighs approximately 45g. The LQ-035Q7DH01 sells for $145 (50).

DROP-IN DISPLAYS

Several vendors offer evaluation platforms that combine the LCD screen, display controller, graphics library, and touchscreen to minimize the development effort. This off-the-shelf approach eliminates the user-interface-hardware development and software integration and allows the designer to add graphics to a device with a simple serial interface. For example, Reach Technology recently announced a 4-in., color, TFT touch-display module for medical, industrial, and gaming applications (**Figure 4**). The company based the 42-0086 display-module kit on the Reach SLCD controller card and a 320×240-pixel LG Philips LCD panel. The unit requires no special operating system or library on the host processor and allows users to access the LCD as an intelligent serial device. The system writes text and graphics images to the display by issuing one of more than 50 high-level commands. Standard features include a variety of built-in fonts, buttons, charts, and meters, along with high-level macro capability. A built-in touch interface allows you to define graphics buttons on-screen; when you push these buttons, they return a serial string. The SLCD microprocessor code includes a graphics library, text fonts, predefined bit maps, and a command interpreter. The 42-0086 module is available as an evaluation kit with a power supply and serial cable for $345 (one).

A display system would be cost-prohibitive for deeply embedded devices; however, you can still create a graphical user interface for such devices. For example, a short-range wireless connection to a general-purpose device, such as a PDA, laptop computer, or mobile phone, can give users a full-graphics display of device operation. Bluetooth, 802.11, infrared, and even a hard-wired connection enable graphical interaction with a much lower development effort and minimal hardware cost. Embedded devices lacking network connections may need no hardware user interface at all. An Internet connection can turn any connected PC with a standard browser into a remote front panel. Plenty of free or low-cost Web-development tools are available to help create a user-friendly interface. With an Internet connection, you can also use the same communications link for remote software updates and product data collection.

As graphics become commonplace in computer and consumer electronics, embedded-system designers must offer similar multimedia features to live up to user expectations and stay competitive. A graphical user interface can often transform a complex embedded device into a simpler, streamlined product with easy-to-update features. With a broad range of off-the-shelf hardware and software products available, designers now have the tools to incorporate a sophisticated graphics interface into ever smaller embedded devices. EDN

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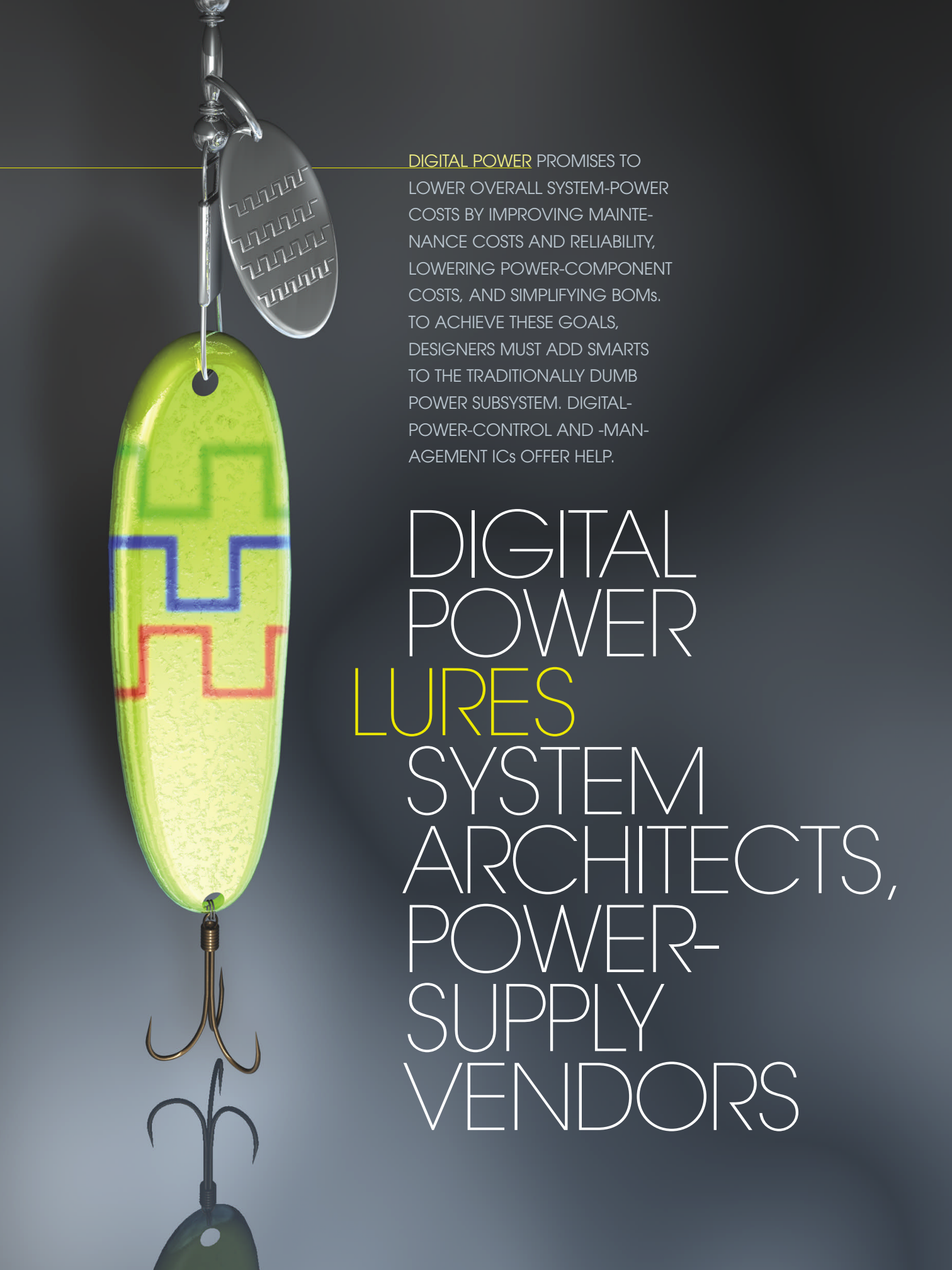
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DIGITAL POWER LURES SYSTEM ARCHITECTS, POWER-SUPPLY VENDORS

BY MARGERY CONNER • TECHNICAL EDITOR



In the past year, digital power has been a hot topic for system architects, power-supply designers, and mixed-signal-IC vendors. Nay-sayers argue that digital power is needlessly expensive and complex—a solution in search of a problem. Proponents argue just as vehemently that digital power is inevitable and will within a few years virtually take over the power-subsystem landscape. These seemingly incompatible viewpoints seem strange for a technology as straightforward as system power, but the disparate views are understandable once you find that each side offers different definitions of digital power and often refers to different applications. This confusion occurs because digital power has two distinct components: digital control of the PWM-feedback loop and power management and communication.

Digitally closing the loop is by far the more complex part of digital power. The first question that springs to mind is: Why use digital control, when SMPSs (switched-mode power systems) do so well with an analog-control loop? Analog-control loops tout accuracy, engineers' understanding of their design, and the support of a plethora of analog-control ICs. However, an analog-control loop targets a specific narrowly defined load. If the load has a wide variation, however, it's difficult to tune the analog loop over the load's entire range. In addition, if you need a design platform that you reuse in a variety of products without changing the parts, analog is a poor match. Says Ron van Dell, president and chief executive officer of Primarion, "If it's a true digital controller, then designers can configure all the aspects of that controller by putting values in registers, using no outside hardware changes." Designers can more quickly optimize and debug the system, working only on a PC's GUI, than they can by soldering and unsoldering various onboard resistance and capacitance values, he says. (For a more detailed explanation of how a digital PWM works, see **Reference 1**.)

Digital-control loops require a relatively fast, powerful processor, which is a drawback in the penny-pinching world of power subsystems. Proponents of digital claim that designers can offset the cost of the processor by eliminating some components or by using cheaper passive components. Says Don Paulus, vice president and general manager of Linear Technology's power-management-product line, "The accuracy with which you generate power is inherently an analog function. However, when you have all this digital capability, instead of making absolutely accurate parts, you can make relatively 'sloppy' parts and then use the digital control to calibrate out a lot of those errors. It's akin to what's happened in signal conditioning, in which you can often make systems that are not very accurate and then calibrate out all the errors."

But performance metrics for power include more than just accuracy, says Paulus. "We're looking at the promise for digital technology to address transient capability," he says. "For example, if the supply knows that a large load step is coming, it could alter its loop dynamics on the fly; respond quickly to that transient; and then shift back to its steady-state, lower bandwidth precision. That kind of flexibility could affect the need for load capacitors." Although interested in digital power, few traditional "silver-box" (closed-frame)-power-supply manufacturers have rushed to switch to it. Only a small slice of Linear's customer base has any interest in digital power, says Paulus.

But digital power involves more than

just digitally closing the control loop. It includes the management and communication functions that are becoming increasingly important in datacom and telecom systems. These systems rely on power processors operating with multiple voltages rails, which must power up and down in a set sequence. In addition to their power-sequencing needs, pieces of equipment such as routers and high-end servers are likely candidates for digital power because of their need to communicate with the system supervisor and their potentially high maintenance costs. The power economy of slightly more efficient digital-control loops is an advantage, but power costs are a drop in the bucket compared with maintenance costs over the lifetime of a supply. As Bob Lukas, product-marketing manager for Intersil's computing-power products, puts it, "A server is defined by its reliability." Digital power may get its first toehold in high-end-computing systems due to its ability to inform the system of the health of the power subsystem with information about current and temperature. Digital-power management can help with reliability and maintenance by reporting temperature changes, unexpected current draw, and fan-speed changes in the power subsystem. All of these factors can tell a maintenance worker more than a simple warning light can.

Chris Ambarian, senior analyst for iSuppli, puts a dollar figure on how the cost of ownership dwarfs the initial power-hardware cost for these huge server and switching farms: For every dollar a power supply costs, the maintenance and cost of ownership is $6. You need not incorporate digital control if all you want are the benefits of digital-power communication and management. Some IC vendors are following the lead of their customers by taking a cautious approach to digital power, reaping the benefits of power management without committing to the added complexity of digital-control loops. Microchip sees the move as gradual and has a road map calling for four levels of integration for digital power, allowing the company to slowly immerse itself into the technology.

AT A GLANCE

- Digital power encompasses both digital control of the PWM control loop and digital-power management and communication. Systems may use one or both forms of digital power.
- Look for several more digital-control and -management ICs to debut this year.
- Expect to see a gradual move toward digital power as processing power grows ever cheaper.

At the simplest implementation, the host system can turn the power subsystem on and off. Keith Curtis, principal applications engineer for the security, microcontroller, and technology-development division at Microchip, says that this capability sounds deceptively trivial but states, "It gives you a number of valuable control options." These options include fault recognition and restart, remote-control start-up, power-up sequencing, and soft start. "This level is very unobtrusive in the analog-loop design," he says.

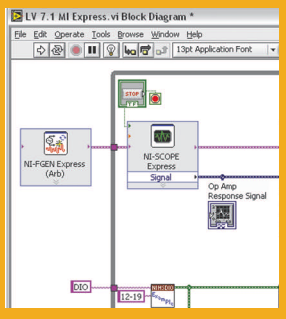


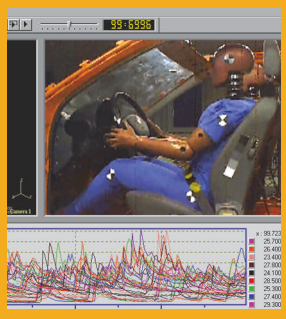
Figure 1 Designers usually dismiss point-of-load supplies as too simple to benefit from digital-control techniques, but this 40A supply from Bellnix incorporates a Volterra digital controller for less than $30.

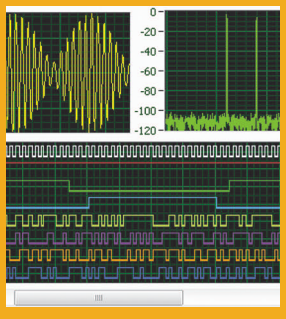
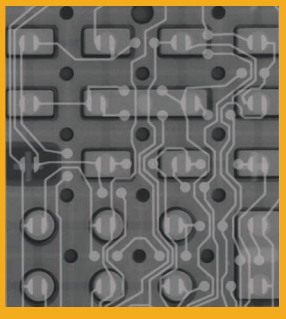
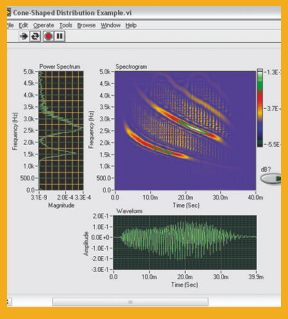
At the next level of complexity, the system power controller controls power-supply outputs and responses. Microchip sometimes calls such designs digitally assisted: The microcontroller is more intrusive and has limited access to some components of the analog-control loop, such as the voltage reference. This level of implementation provides a true soft start, because you can control the output voltage, and requires an inexpensive microcontroller, such as Microchip's PIC10, which sells for less than 50 cents (volume quantities). The addition of a microcontroller enables such features as undervoltage lockout, delayed start-up, and clock dithering in a SOT-23-package microcontroller and eliminates the cost of implementing these features in separate circuits. Adding a microcontroller also allows you to support digital-communication functions through a protocol such as the PMBus, an industry-backed standard, which its developers based on the hardware-standard I^2C bus (**Reference 2**). This level of implementation is popular for designers hesitant about committing to a pure-digital-power design. Ahmad Ashrafzadeh, business manager for digital-power products at Maxim, says, "For most designers interested in digital power, closing the loop is not first on their list; it's nowhere near the top." Instead, he says, they want features such as the ability to control the output voltage; to track, sequence, and get feedback on parts; and to use these diagnostics to track the health of the overall system. Maxim plans next month to introduce a chip that achieves these goals and works in tandem with an analog PWM-controller IC.

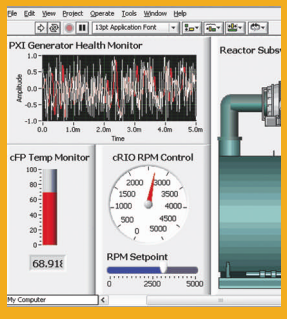
Microchip's next level of implementation still relies on a traditional analog-feedback loop but allows the microcontroller to modify the power supply's topology, such as in an application for an LED flashlight with a rechargeable battery. The battery charges from a buck topology and discharges from a boost topology. Such a circuit can use the same—yet differently configured—inductors and capacitors and reconfigure from a buck supply charging the battery to a boost supply discharging the capacitor into the supply lines. To date, only Microchip offers a microcontroller, the PIC16F785, that targets this level of integration.

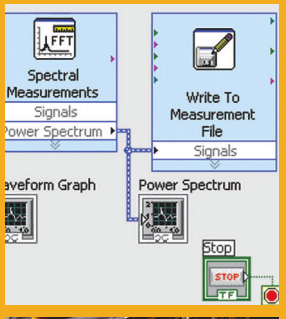
Microchip's highest level of implementation, true digital control, integrates all the PWM-control loops into a digital controller. Much activity has occurred in recent months in this area. Last summer, only Texas Instruments, with its UCD9k and UCD7k DSP-based chip set, and Silicon Laboratories, with its Si8250, had

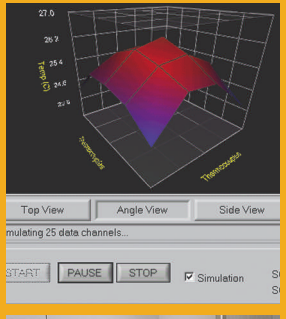




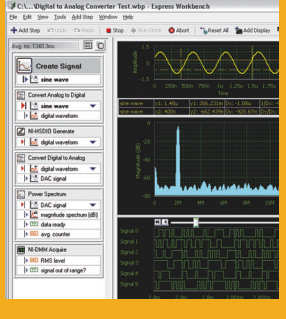



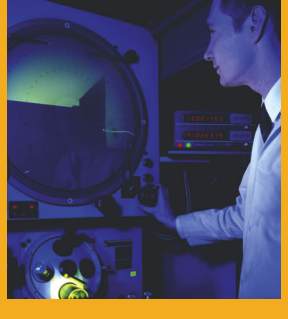
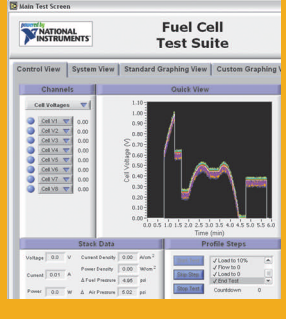
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announced such products. Since then, Primarion has introduced the PX7510 for POL (point-of-load)-system applications, Zilker Labs has introduced the ZL2005, Linear Technology has announced that it is acting as a second source for Primarion's POL chips, and Intersil has announced its second-sourcing of Primarion's PX3535 part for motherboard core voltages. In addition, expect competing chips from Analog Devices, Microchip, and Texas Instruments by the end of the third quarter of this year.

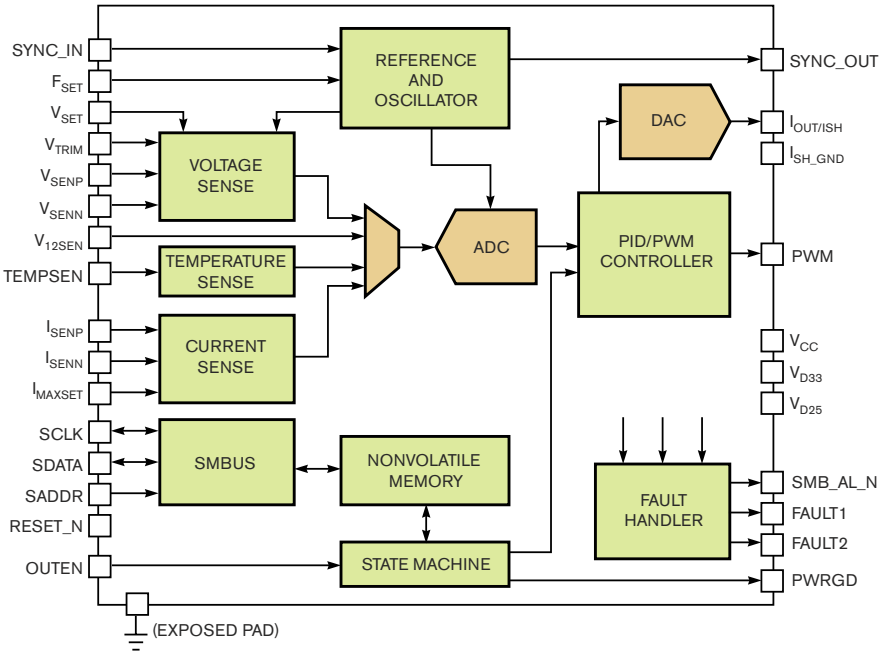
With the exception of the UCD9k and UCD7k from TI, all of these chips have moved away from the fully programmable, general-purpose-DSP model to the more streamlined, dedicated-state-machine/digital-filter combination. Even so, the amount of software configurability available for these chips varies considerably, ranging from Zilker Labs' almost completely hard-wired ZL2005, which sets loop and performance characteristics by pin-strapping inputs to the chip, to the Silicon Labs approach, in which the system uses an 8051 core to perform communication tasks. All the manufacturers have configured the chips with GUIs that hide all digital-loop-control algorithms from designers. Prices for the chips range from $1.50 to $5.

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Despite the rush of interest by IC vendors, dedicated ICs will not necessarily dominate digital control. Lambda Power's R&D experience with digital controllers serves as a real-world case study of how to evaluate new technology when you're trying to anticipate your customers' needs. Hiroyuki Yashiro, chief technical officer of Densai-Lambda, the sister division of Lambda Power in Japan, says that the company has R&D efforts in three divisions, each designing converter applications: a dc/dc converter, a UPS (uninterruptible power supply), and an ac/dc converter. Each design group independently selected its control chips: a general-purpose TI DSP chip, a custom ASIC, and an Atmel FPGA, respectively. Why does Lambda consistently go the roll-your-own route? Eiji Takegami, a design engineer with Lambda's advanced-development department, says, "Customers won't buy a power supply if the performance is equal to an analog-loop-based supply; the performance must be better." Takegami cites the fact that a digital-control loop can respond to a wider range of capacitive loads and still stay within spec than can an analog loop.

In addition to superior performance, Yashiro cites the benefits of having one standard platform as both cost-saving and flexible. Designers must make changes through software rather than manually tweaking, redesigning, or swapping out components. Another reason for developing the control circuitry in-house is the importance of differentiating products. Although some vendors want to make the digital-control-loop design as painless as possible, Lambda sees the turnkey approach as a drawback—that is, if anyone can design a digital-control loop, what value does Lambda add to the process?



Primarion's single-phase, step-down, PMBus-compliant PX7510 digital dc/dc converter, which Linear Technology will sell as the LTC7510, provides for outputs as low as 0.7V. The price is $1.75 (1000).

WHAT'S AHEAD?

Most power subsystems currently offer simple on/off communication ability, so it will take a while before a sizable percentage of systems relies on any form of digital power. High-performance processors now have limited ability to manage power, but that ability is vital for the coming breed of electronics, says Shekhar Borkar, a fellow and director of microprocessor research at Intel. He describes chip power as having two components: delivery and dissipation. "You've got to improve your performance in the envelope that you can afford with the power delivery and power consumption," he says. "How can you improve the processor performance in that power envelope? The answer is: Put a lot more processing power into it." In the past, processing power, rather than electrical power, limited designers' abilities in this area. Moore's Law makes transistors plentiful, and Borkar has exploited the surfeit of

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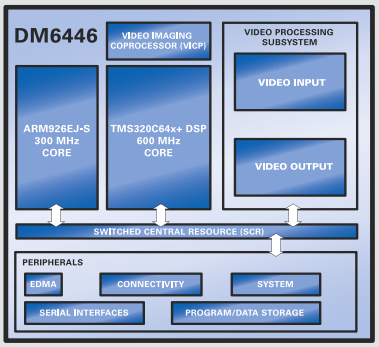


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VC1/WMV 9 Encode	D1+	n/a
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transistors to put the power digital-control loop under the control of the server's processor, saying that some of the company's products incorporate digital power. Borkar predicts that the trend of having the main processor control digital power will trickle down into mainstream products, such as laptops and desktop systems (**Reference 3**).

In addition to processor power, system architects must also be able to manage power at the system level. Energy-saving mandates that focus on power-supply efficiency, such as EnergyStar, are important, but they look at only part of the picture. For example, in a cell-phone transmitter/receiver system, the radio base station accounts for more than 90% of the power consumption for a network, including the handsets and their power conversion (**Reference 4**). Making cell phones' ac/dc and dc/dc converters more efficient is one step toward managing power, making the devices approximately 1% more efficient. However, because the radio base stations themselves are relatively efficient, increasing the converters' efficiency by this percentage does not significantly impact the devices' overall efficiency. Pierre Gildert, an engineer at Ericsson Microwave Systems, points out: "The closer you get to the antenna, the more expensive the losses become." Thus, you can achieve great power savings by putting the remote-radio unit on the antenna tower and enabling it to respond dynamically to power fluctuations. For example, the system would benefit from a sleep mode, which requires intelligence, on/off control, and fast response for wake-up, as well as the intelligence to adapt to low- and high-traffic periods.

Ambarian of iSuppli predicts that the next step in system-power management will require the establishment of a POS (power operating system), which will rely on power-subsystem drivers to communicate. These drivers can be silver-box power supplies, voltage-regulator chips, or POL converters. The POS will allow system designers to manage every aspect of a given power system, on time scales that are appropriate to every level of a control scheme. Those time scales will range from nanoseconds to seconds, and Ambarian predicts that comprehensive control of them will provide benefits in system efficiency, flexibility, and reliability.

Don't count out the lower end of power subsystems from the future of digital power. Bellnix, a maker of POL converters for FPGA-based systems, recently introduced its 40A BDA series of POL converters with PMBus interfaces. The small module sells for $30 and uses the Volterra digital processor (**Figure 1**). Power-One has started offering Z-1000 No-Bus digital POL converters, such as the 15A ZY1015, which require no external communication overhead. EDN

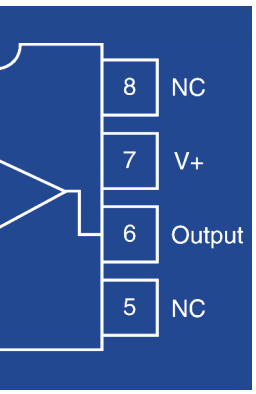
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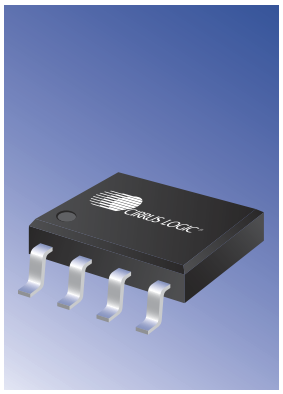
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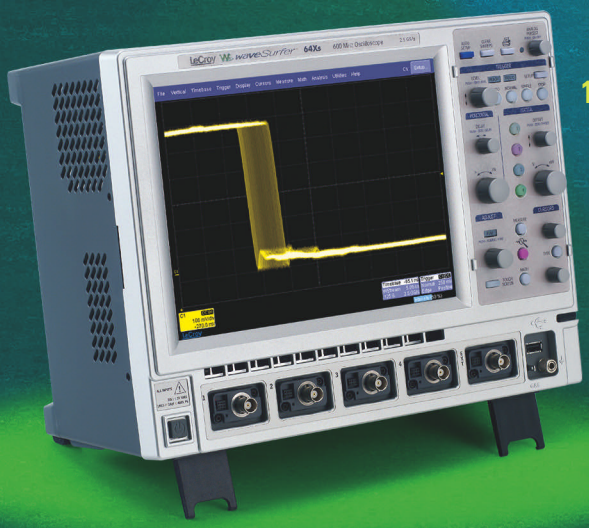
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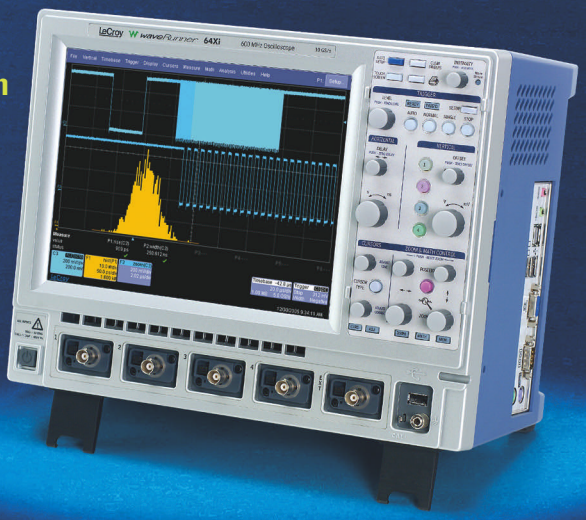
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Dynamic packet classification enables multimedia traffic on WLANs

RETHINK YOUR QOS IMPLEMENTATION TO ENSURE THAT YOUR DESIGN CAN HANDLE WIRED AND WIRELESS CLIENTS.

Network-switch designs have evolved to support multimedia traffic through QOS (quality-of-service) techniques. But WLANs (wireless LANs) fundamentally differ from wired Ethernet in a number of ways and particularly in that clients roam among access points. So, wired-Ethernet QOS measures don't apply seamlessly to WLANs. A designer can rethink the QOS implementation, and particularly how to implement COS (class-of-service) queues to ensure that a switch handles wired and wireless clients equally well in the case of rich data streams.

In multilayer switching that supports QOS, the processing at the switch egress mainly focuses on the scheduling of the exiting packets. Packets reside in various COS queues before the network schedules them for forwarding. The assignment of the COS depends on either the examination of the packet content or the priority that comes with the packet.

In a wired-QOS scheme, each egress port has a fixed number of COS queues, because the downlinked, wired, end-client devices connect directly to the switch. A wired-client device rarely hops from one switch port to another. Clearly, binding COS queues to an egress port can be a major drawback in an enterprise network with WLAN support. Typically, a WLAN-client device connects to the enterprise-LAN infrastructure through an access point, but the connection to that access point is not permanent. The wireless client can move from one location in the office to another, thus changing the connection point in the enterprise LAN from one access point to another. Assuming that two access points connect to the same switch, when an access point hands off the wireless connection to another access point, the sudden change of exiting packets from one egress port to another would present a problem. Because the exiting packets queue up at one egress port, the movement of the client device to another access point and egress port would prevent the queued packets from reaching the intended client, resulting in either packet loss or retransmissions, depending on the application.

An enhancement of egress-queue management can accommodate mobility in wireless applications, particularly latency-sensitive applications such as VOWLAN (voice over WLAN). In this enhanced method, the COS queues do not depend on

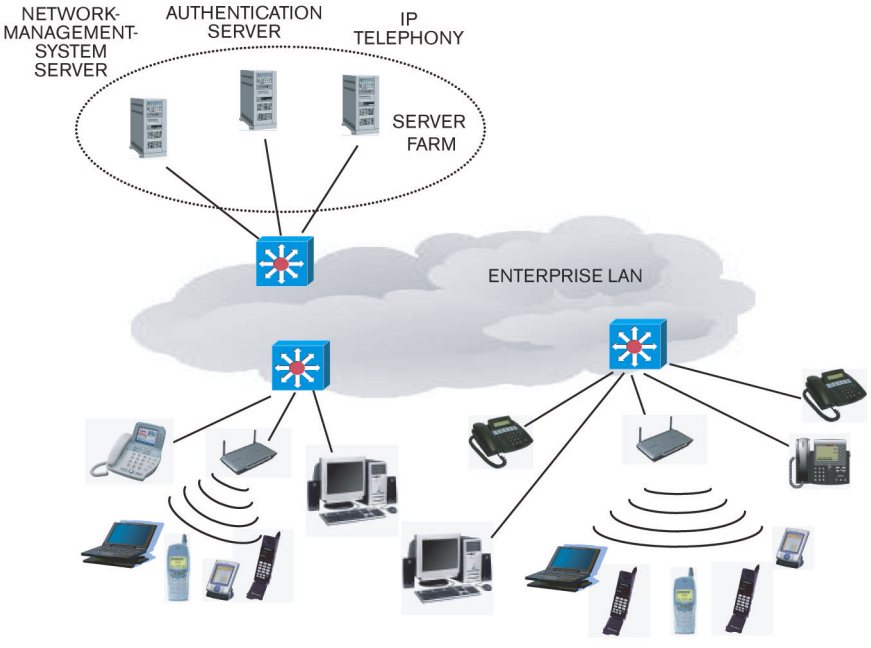


Figure 1 Next-generation enterprise networks will require unified accessibility for both wireless and wired clients, as well as convergence of voice and data applications.

the physical egress ports as in legacy switches. You can consider each COS queue as a flow of packets traveling toward a client. Because each COS queue dynamically binds only to a physical port, you can easily modify the binding when the client device moves from one access point to another. The COS-queue bindings are software-programmable, based on the establishment, tear-down, and predetermined idling time-out of traffic flows.

UNIFIED ACCESS IN THE ENTERPRISE

Consider the case of VOWLAN—essentially, VOIP (voice over Internet Protocol) over a WLAN—as it emerges as a key enterprise application. Next-generation enterprise networks will require unified accessibility for both wireless and wired clients, as well as convergence of voice and data applications (**Figure 1**). In an enterprise environment, devices such as PCs, servers, wired IP phones, and access points can connect to the switch. The access points in turn cover WLAN devices, such as WLAN-phone handsets, PDAs, and laptops.

Challenges such as security, network reliability, and QOS were obstacles to IP telephony even in wired LANs. But current intelligent, multilayer, wired, or legacy switches have adequately addressed these issues. In legacy switching, ingress-packet filtering and egress scheduling are the usual mechanisms to enable QOS for latency-sensitive traffic. The most important concept in intelligent switching is the concept of a flow, which represents all the packets of a source, destination, application protocol, traffic characteristic, or a combination of all these criteria. Traffic that constitutes a flow can be, for example, a media stream from station 10.5.98.2 at port 31320 to station 10.5.92.102 at port 56020, with UDP (User Datagram Protocol) as the Layer 4 protocol. (The common ingress filtering is the source-IP address, destination-IP address, Layer 4 protocol, source Layer 4 port, and destination Layer 4 port.) Other examples of flows are ones including all packets between station 192.168.93.10 to 192.168.22.0/24, all HTTP traffic originating from 10.5.8.22, and all traffic originating from 192.168.112.0/24 with a DSCP (differentiated-services code point) of seven, etc.

A legacy switch uses its ingress-filtering capability to identi-

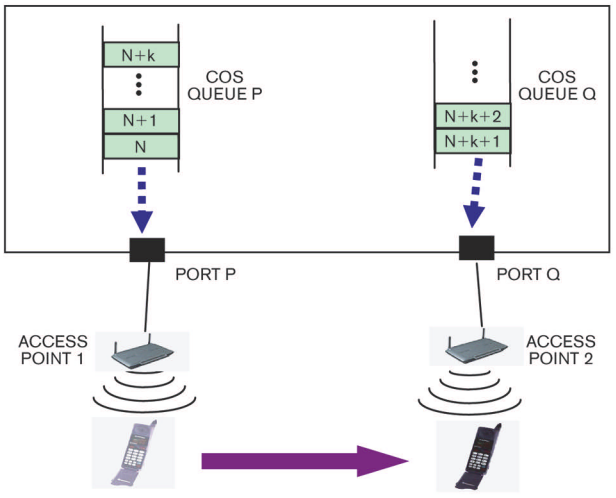


Figure 3 Statically bound queues to egress ports in a mobile environment have limitations.

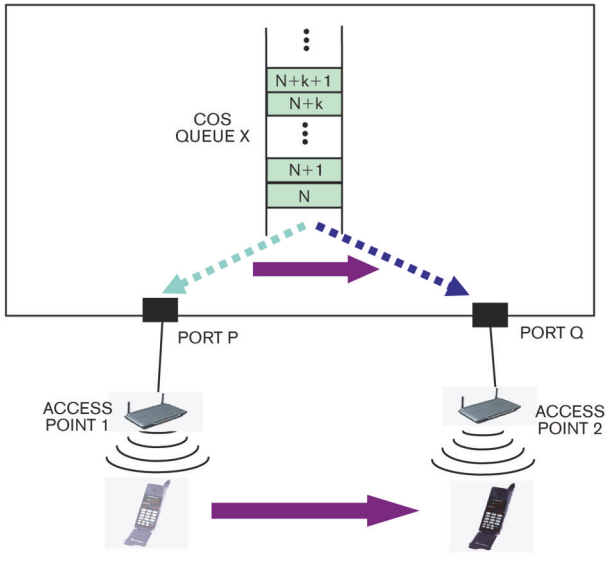


Figure 4 In this scenario, packets still queue up at COS X without jumping from queue to queue.

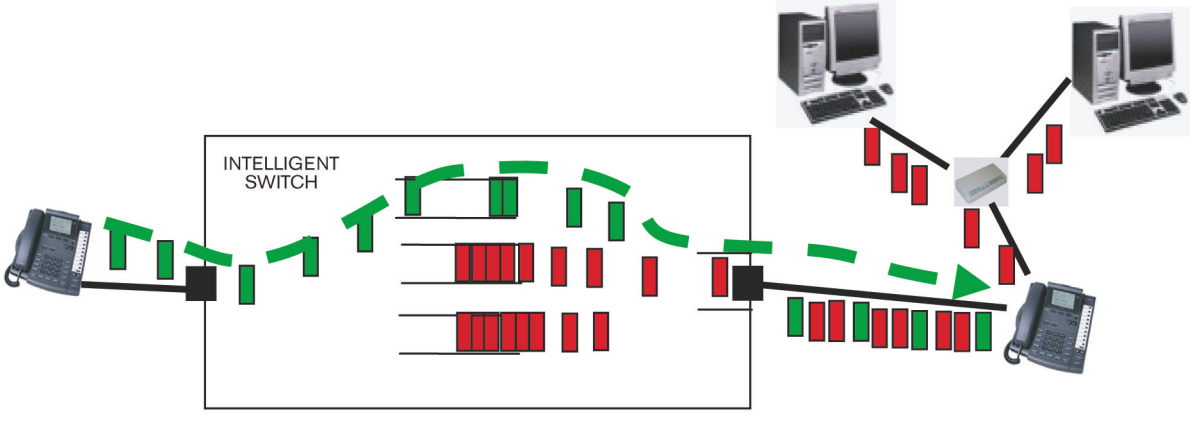


Figure 2 In a legacy switching operation, a single wire drop goes from the wiring closet to the end-user office or cubicle, in which the user connects both the voice- and data-network equipment.

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fy the traffic and classify the packets into certain flows that the network administrator defines to have the traffic conform to certain data-forwarding profiles. The resulting actions of packets in flows include dropping the packets, policing or shaping the traffic to a certain bandwidth requirement, assigning internal COS for the packets, and redirecting or mirroring the traffic to other destinations. After the ingress filtering of a packet, the switch identifies the packet's egress ports. It then places the packet in the COS queue of its designated egress port for forwarding. The scheduling of packet exits depends mainly on the packet's internal COS and the flow's bandwidth profile. The common scheduling algorithms include strict priority, weighted round robin, and weighted fair queuing. In most legacy switches, each egress port has a predefined number of COS queues—commonly, four or eight—to accommodate the classified packets. The network administrative traffic, latency-sensitive application traffic, and mission-critical application traffic usually get higher COS. Because VOIP applications are latency-sensitive, the packets associated with those applications' voice and video flows usually receive higher COS numbers within the switch.

In egress scheduling in a legacy-switching operation, a single wire drop goes from the wiring closet to the end-user office or cubicle, in which the user connects both the voice- and data-network equipment—that is, an IP phone and two PCs—to one Ethernet jack (**Figure 2**). The voice packets are in the higher COS queue and, hence, take precedence over latency-insensitive traffic traveling to the PCs in the exit scheduling.

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NEW CHALLENGES IN VOWLAN

Though legacy ingress-filtering and egress-scheduling schemes work well in wired-LAN clients, VOWLAN presents a new technical challenge in intelligent switching. The movement of wireless-client devices is common in VOWLAN because these devices migrate from one port of a switch to another as they hop from access point to access point. Placing a client's packets at a COS queue of a certain egress port presents a problem if the client is moving from one access point and one egress port to another access point and egress port. Legacy switches don't typically dequeue packets from the COS queue of one port and place them in the COS queue of another port. Because packets have queued up at one egress port, they will transfer to the port's connected access point and be unable to reach their intended client. A WLAN infrastructure with old access points further emphasizes the need for better queue management, because these access points have little buffer space. Therefore, most of the downstream frames for the clients must queue up at the switch.

Statically bound queues to egress ports in a mobile environment have limitations (**Figure 3**). After packets N, N+1, and so on, through N+k are in the egress queue, the client moves from one access point to the second access point, effectively changing its connection to the LAN from Port P to Port Q. As packets for the client start accumulating at the COS queue, these remaining packets still arrive at the first access point and transmit through the air to a client that has roamed away. The problem stems from a lack of a well-defined mechanism to dequeue packets N, N+1, through N+k at COS P and place them at COS Q. Furthermore, these dequeued packets must jump in the line at COS Q because they should arrive before packets N+k+1, N+k+2, and so forth. Unfortunately, such egress queuing with mobility knowledge is uncommon in legacy switches.

For non-real-time, wireless-data applications, maintaining session persistence is not the most critical issue. For example, if you are downloading a large file on your laptop while moving with it around the office, the TCP (Transmission Control Protocol) session can always retransmit the lost packets, because FTP (File Transfer Protocol) is not a real-time, latency-sensitive application. On the other hand, latency-sensitive VOWLAN has more stringent requirements and demands seamless hand-off between one access point and another when the wireless handset moves around the office. Otherwise, the network may interrupt or drop the conversation. The infrastructure should avoid both long latency for executing the hand-off and packet losses resulting from the hand-off.

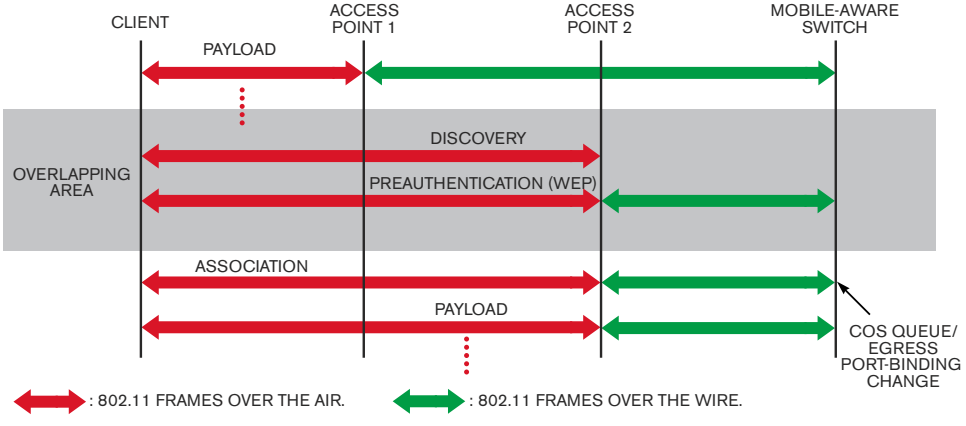


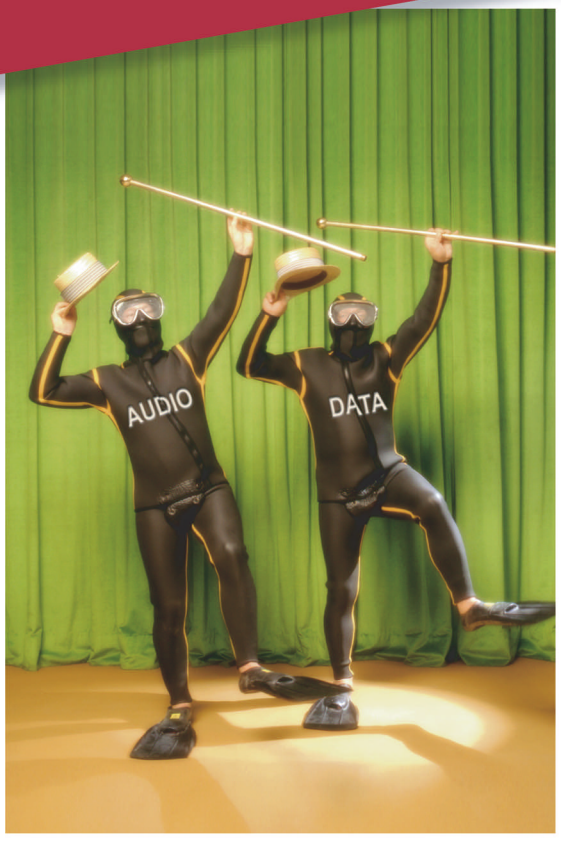
Figure 5 The most crucial step of this hand-off scenario is the change of COS queue to egress-port binding at the switch.

CENTRALIZED QUEUE

The solution to the seamless-mobility problem centers on another type of COS queues to egress-port binding. Obviously, designers must revise this scheme of static binding of COS queues to egress ports for mobile-aware switching. A flexible, dynamic association of COS queues to the egress ports constitutes the core concept of this approach. This sce-

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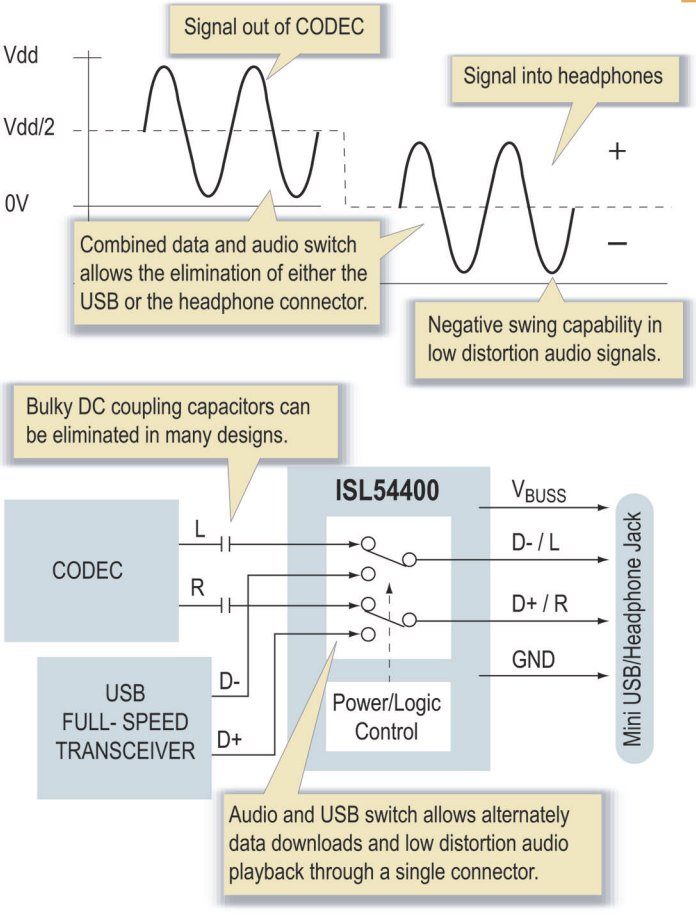
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nario involves a centralized pool of egress-COS queues in the switch. The centralized pool allocates the COS queues on demand as soon as you set up a flow for ingress filtering of the voice stream. The COS queue logically binds only to the egress port that links to the IP phone. For wired-IP telephony, this binding remains the same for the duration of the call. For wireless-IP telephony, this binding is subject to change as soon as the mobile client moves to another access point.

Queue COS X handles the flow of downstream packets to the wireless handset (**Figure 4**). Packets accumulate in this COS queue, which initially binds to egress Port P. After the client hops from Access Point 1 to Access Point 2, thus changing its association to the switch from Port P to Port Q, the binding of COS X to Port P simply reconfigures to Port Q. In this scenario, packets still queue up at COS X without jumping from queue to queue.

In a typical access-point-hand-off situation, the WLAN phone gradually moves from the coverage area of Access Point 1 to that of Access Point 2 (**Figure 5**). The most crucial step of this hand-off scenario is the change of COS queue to egress-port binding at the switch. In this example, you must assume that the WLAN-phone handsets, like most such products on the market, support WEP (wired-equivalent-privacy) encryption and preauthentication; that the switch handles most of the 802.11 processing; and that the access points are thin, handling functions such as beaconing, power management, and over-the-air QOS. Further, you must assume that the switch software performs some of the mobility processing, such as preauthentication and association; that the access point does not transform 802.11 frames to 802.3 Ethernet frames or vice versa; and that an encapsulation tunnel exists between the switch and the access point to transmit the 802.11 frames, which the switch processes. You must also assume that the WLAN phone is initially associated with Access Point 1; thus, the voice packets between the client and the switch transmit through Access Point 1.

To move the client from Access Point 1 to Access Point 2 involves three steps. The first two steps, discovery and preauthentication, can take place within the overlapping area of the two access points. Once the client exits the coverage area of Access Point 1, the client, Access Point 2, and the switch complete the move with Step 3: association. The software in the switch registers the association between the client and Access Point 2 and then triggers a new binding of COS Queue X from Port P to Port Q. This reconfiguration of the queue thus redirects to Access Point 2 all the packets that should transmit to Access Point 1. The dynamic binding mechanism ensures no packet loss in the switch due to the hand-off.

To deploy VOWLAN, you must enhance the enterprise-LAN infrastructure to accommodate the various technical challenges of wireless-networking and voice applications. The key technical challenges include mobility and session persistence, traffic management, location awareness, and security. The LAN infrastructure must be able to support movement of wireless clients with seamless hand-off of latency-sensitive flows. Traffic-management capabilities must include QOS, differentiated services, bandwidth guarantee, and rate policing and shaping traffic of various priorities. Location awareness is important for several reasons, including support for advanced preauthentication and load balancing. This feature is also crucial in pinpointing a client device in the case of an emergency, particularly in a large enterprise premise. Currently, VOWLAN clients in the market use WEP as the security measure, but future designs may require 802.11i support. EDN

AUTHOR'S BIOGRAPHY

Edward Lor is a senior application engineer at SiNett Corp (www.sinett.com). Before joining SiNett, he was the chief architect in the wireless-communications group of Hong Kong's ASTRI (Applied Science and Technology Research Institute). Lor has also held various design, technical, and project-lead positions at Broadcom Corp and Lucent Technologies. He has extensive experience in IP telephony, VOIP security, and wireless-LAN and multilayer networking. Lor received his doctorate in computer science from the University of California—Los Angeles.

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BY RAVI CHANDRAN • FREESCALE SEMICONDUCTOR

Power dissipation in high-end integrated communication processors

ARM YOURSELF WITH TOUGH QUESTIONS FOR CHIP VENDORS TO MORE ACCURATELY COMPARE POWER AMONG PROCESSORS.

Traditionally, chip vendors' hardware specifications have provided typical and maximum core-power values at various frequencies. A common engineering practice has been to use the typical power number for thermal design and the maximum power number for power-supply design, adding appropriate margins to account for I/O power.

However, with the advent of high-end integrated communication processors, engineers must pursue this practice with some caution. The definitions of "typical" and "maximum" power are not standard. Surprisingly different definitions may arise among vendors as they tout "marketing-optimized" power numbers in an increasingly power-sensitive embedded-system marketplace. Voltage, temperature, and application are among the obvious factors that may differ in power specifications, but other more subtle differences may also exist. Profiling power on an arbitrarily selected part may provide misleading results. The imminent introduction of standardized power benchmarks, such as EEMBC (*EDN* Embedded Microprocessor Benchmark Consortium) EnergyMark, is an attempt to standardize many aspects of the measurement conditions. Unfortunately, these standardized benchmarks can also produce misleading results (see **sidebar** "Issues with power benchmarks").

SOURCES OF POWER CONSUMPTION

"Power dissipation," or "consumption," refers to the power that various power-supply rails deliver to a processor for proper device operation. The cooling system must remove this power to ensure that the processor-die-junction temperature remains within the recommended operating conditions.

Discrete processors usually have separate sets of power-supply pins for the core, the I/O interface, and the PLL (phase-locked loop). The I/O and PLL supplies together usually account for less than 5% of the total power of the processor. Note that "core" refers to not only the CPU, but also all other internal circuitry, such as cache, memory, interconnect circuitry, and various other logic blocks.

Integrated communication processors have one or more integrated memory controllers, as well as a plethora of I/O interfaces and hardware-acceleration blocks. Hence, the parts usually provide additional sets of power-supply pins, either because the voltages that the I/O requires differ or to provide better isolation between interfaces. Several separate PLL supplies are also common for supporting independent interfaces. Depending on the I/O interfaces you use, the I/O supplies typically consume 10 to 20% of the total device power.

WHAT POWER DATA DO DESIGNERS NEED?

Designers need to know the worst-case power dissipation on each supply rail so that they can design the power supply to provide the required peak current. Inadequate current supply on a rail during peak-current draw may cause the voltage to droop on that rail and ultimately result in system failures that can be difficult to trace.

The thermal design must account for the total power dissipation of the device. Ideally, you could design the cooling system to remove power equal to the sum of the worst-case power consumption on each supply rail. However, in today's designs, this goal can be challenging to attain and may be unnecessary.

The power that most realistic applications dissipate varies over time and may vary among supply rails. The cooling system need not remove instantaneous peak-power dissipation. It is usually reasonable to have a cooling-system design that removes average power dissipation over milliseconds or seconds depending on the application and the overall margin available. Failure to provide adequate cooling may not result in immediate failure, but it could affect the long-term reliability of the device, surrounding devices, and possibly even an entire chassis-based system.

Finally, a system designer needs power-dissipation information from various vendors to make comparisons. After narrowing the processor choices to those devices that can fit within the maximum power budget of the application, a designer has to consider relative power metrics. Power dissipation and performance per watt of representative applications are the common metrics designers employ. Designers may have to extrapolate power data from vendors to achieve a fair and valid comparison (see **sidebar** "Quizzing chip vendors on power").

DYNAMIC AND STATIC POWER

Particularly with smaller process geometries, it is important to understand that you can separate core power conceptually into two main components: dynamic power and static power. You can express this relationship simply as: core power=dynamic power +static power.

Dynamic, or "ac," power, arises due to transistor switching activity; a device consumes power when internal load capacitances charge or discharge with logic-level changes. If you turn off the clocks, dynamic power is zero. Dynamic power varies lin-

early with frequency and depends on the software running on the device. It also varies quadratically with core voltage. Often, within the same process technology, a vendor may specify higher core voltages for higher frequency ranges. Note that dynamic power is independent of junction temperature. In summary, you can express dynamic power, D, as: $D=kAV^2F$, where A is an activity factor that depends on the software, V is the core voltage, F is the CPU frequency, and k is an empirically determined constant.

Most communication processors contain at least two major frequency domains, one for the CPU and the second for the platform; the platform bus typically runs at twice the speed of the DDR (double-data-rate) memory clock frequency to match the DDR. Hence, it may be useful to think of the dynamic-power behavior as composed of two independent terms:

$$D=k_1A_1V^2F_{CORE}+k_2A_2V^2F_{PLATFORM}.$$

Static, or "dc," power refers to power dissipation that occurs as long as the part is on, even if the clocks are off. It is due to the flow of leakage current that occurs in every powered transistor. It depends on core voltage and junction temperature.

Some use the term "sleep power" synonymously with static power. When you place a part in a power-saving sleep mode, most of the device is off. However, some parts of the device, such as the interrupt controller, are still on so that an interrupt can wake the device. Hence, sleep power has a small frequency dependence and would be higher than the static power under identical temperature and voltage conditions. But, in most cases, the difference between sleep and static power is likely to be negligible.

Unlike dynamic power, static power lacks a common simple expression to describe its variation with core voltage and junction temperature. But static power increases exponentially with junction temperature. In fact, it could possibly even double over a 40 to 50°C temperature change in a 90-nm process. For its variation with voltage, it is reasonable to assume that static power increases quadratically with voltage, similar to dynamic power.

Figures 1 through **3** qualitatively illustrate average core-power variation with core frequency for a typical processor. **Figure 1** shows that, when you keep the application, core voltage, and junction temperature of a device the same, the average core power varies linearly with core frequency. When you change only the temperature and keep all other conditions the same, you can obtain parallel lines for the core-power variation with the core frequency for each given temperature. The y intercept of each line represents the static power of the device at a particular core voltage and junction temperature.

In **Figure 2**, the application and the junction temperature are the same in all cases. For each given core voltage, the average core power varies linearly with core frequency. However, when you use a higher voltage, the line has a higher slope as well as a higher y intercept (higher static power). The slopes increase with voltage, because dynamic power has a quadratic variation with voltage, and static power generally also increases exponentially with voltage.

The distinction between static and dynamic power may be interesting in itself, but what is its value to a designer? First, as designers use faster process technologies to achieve speeds close to and above 1 GHz, the proportion of total power that is due to static power increases significantly from low single-digit percentages to significant double-digit percentages.

Second, static power can vary significantly from part to part, and dynamic power exhibits little variance across parts using the same manufacturing process. With such significant part-to-part variations in power dissipation, measurements you make on one part do not necessarily indicate the worst-case power scenario for all parts. Underestimating processor power through failing to account for worst-case static power when designing cooling systems could have serious consequences as it may impact device reliability.

Third, designers should note that power may differ among parts from different frequency bins even under otherwise-iden-

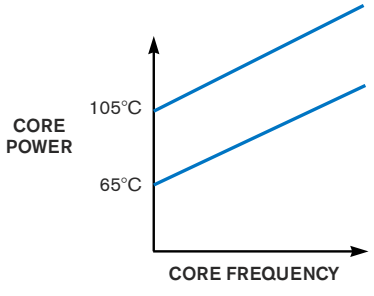


Figure 1 The average core power varies linearly with core frequency when the application, core voltage, and junction temperature are constant. When you change only the temperature, you can obtain parallel lines for the core-power variation with the core frequency for each given temperature. The y intercept of each line represents the static power of the device at the particular core voltage and junction temperature.

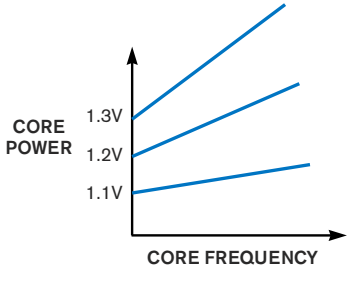


Figure 2 For each given core voltage, the average core power varies linearly with core frequency. However, when you use a higher voltage, the line has a higher slope, as well as a higher y intercept, indicating higher static power. The slopes increase with voltage because dynamic power has a quadratic variation with voltage, and static power generally also increases exponentially with voltage.

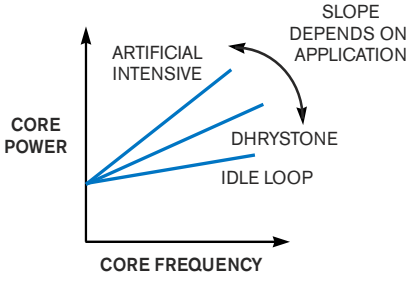
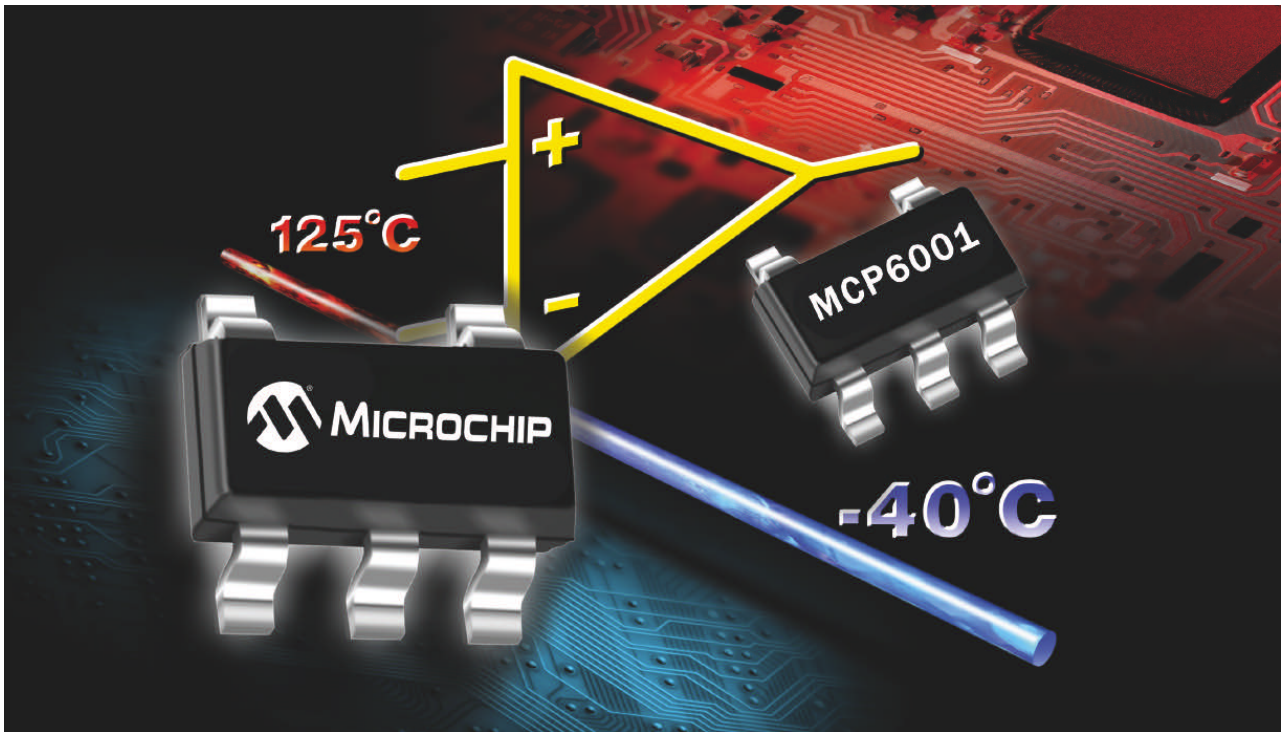


Figure 3 In this figure, the core voltage and junction temperature remain constant for different software loads. The slope varies for different kinds of applications, with an artificially designed application to maximally dissipate power having the highest slope, an idle loop having the gentlest slope, and a Dhrystone benchmark having a slope between these extremes. The y intercepts of the lines, which indicate the static power of the device, coincide, because static power does not depend on the software.

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tical conditions. This situation occurs because a part that runs at a higher frequency generally tends to have higher static-power dissipation. When a designer decides to lower the frequency of a device that a vendor specified to operate at a higher frequency, it may actually dissipate more power than an identical device that the vendor specified for operation only at the desired lower frequency. Thus, it is important when going to production to obtain devices that vendors specify for the desired frequency of operation and not something higher; lower frequency devices may also be lower in price. Also, note that even within a frequency bin, static-power variations occur from one part to another due to process variations.

Fourth, in some power-conscious system designs, clocks are gated to a device or board to save power during periods of lower system-level usage. A similar situation but on a smaller level involves placing a processor in a power-saving sleep or nap mode; this approach is especially useful for EnergyStar compliance during idle periods in products such as printers. In such situations, the device still consumes static power, and you should take into consideration its temperature dependence to determine the actual power savings during idle periods.

Finally, when a hardware specification provides core power and sleep power, you can separate the core power into its dynamic and static components, because sleep and static power should be close. However, sleep power usually occurs at a lower temperature than the core-power specifications, which vendors must convert to equivalent temperatures to accurately separate the components.

HOW SOFTWARE AFFECTS POWER

Software can significantly impact dynamic core power, which usually varies over the course of an application. Thus, for thermal system design, a designer has to consider the kind of code present in the software and the duration for which any high-power code runs to determine the appropriate thermal design.

Figure 3 qualitatively illustrates how the average core power

ISSUES WITH POWER BENCHMARKS

Power benchmarks are still in various stages of development, and not all details of the measurement and certification process are available. However, difficulties arise in using power benchmarks for high-end integrated communication processors that require heat sinks.

STATIC POWER: Benchmarking certification usually involves measurements on a single instrumented board for the benchmarked processor. This certification is adequate for performance benchmarking, because devices of the same kind at the same frequency should produce the same performance results under identical stimuli. However, the power dissipation of high-end processors varies from one device to another due to static-power variation even under otherwise-identical conditions. Static power in high-end devices reaching 1 GHz and beyond in 130-nm and smaller process geometries can account for a significant portion of the total device power. The use of a single device to benchmark power may provide misleading results.

COOLING SYSTEM AND TEMPERATURE: Development boards in a benchmark-certification process usually do not represent customer board designs from a cooling-system perspective. For instance, a heat-sink fan in a development board usually keeps the device well below the maximum operating temperature. However, high-reliability systems do not use heat-sink fans due to long-term reliability requirements. Instead, they typically use passive heat sinks together with redundant cooling systems, and the resulting systems are more likely to operate close to the processor's maximum operating junction temperature. Because static power varies exponentially with temperature, the results depend ultimately on the junction temperature at which the device under test settles.

Even if the benchmark-test results provide the power consumption of the active cooling system, the results may not be useful unless the designer plans to use a similar active cooling system under the same ambient-temperature conditions.

INTEGRATED PERIPHERALS: Benchmarks are generally limited to exercising the core and the memory interface. However, highly integrated devices offer a variety of on-chip peripherals–from Ethernet ports to PCI interfaces. These additional features are not in use, although they continue to consume static and possibly some dynamic power if you leave them on during the benchmark run. Thus, a communication processor with fewer features (and a correspondingly smaller die) is likely to consume less power than one with more integrated features.

Benchmarks generally serve two main purposes for system designers: They provide certified information on absolute performance under known conditions, and they provide a means of comparing competing devices. Unfortunately, power benchmarks are unlikely to satisfy these purposes in the case of high-end integrated communication processors.

You cannot use absolute power numbers from benchmark results for design purposes; you must consult vendor data sheets for thermal and power-supply design guidelines.

Relative comparisons of power-benchmark results of competing communication-processor vendors are unlikely to be reliable, due to differences in cooling systems, processor static-power variations, integrated-peripheral composition, and the benchmarks that do not exercise these peripherals.

Furthermore, even comparing the relative power of benchmark suites on the same processor can be misleading, because the relative results depend on the static power of the processor you use.

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varies with core frequency for a typical processor; the core voltage and junction temperature of the device are constant while different software loads run. The slope varies for different applications: an artificially designed application that maximally dissipates power having the highest slope, an idle loop having the gentlest slope, and a Dhrystone benchmark having a slope between these extremes. The y intercepts of the lines, which indicate the static power of the device, should all coincide, because static power does not depend on the software.

Cache-resident code that executes in tight loops with few incorrectly predicted branches generally dissipates higher dynamic core power. Low-power code tends to have more pipeline stalls, resulting in execution-engine starvation, and it typically involves many loads and stores to main memory.

Examples of high-power code include voice- or image-signal processing, compression, and encryption software algorithms. Such code can often take advantage of superscalar architectures and any available vector SIMD (single-instruction-multiple-data) units. The benefits of such vector units usually far outweigh the associated increase in power, because the device attains its performance boost without increasing frequency and core voltage. For instance, one experiment ran 20 EEMBC benchmarks from the Networking and Telecommunications benchmark on a Freescale PowerPC 7457 processor with and without the use of its Altivec vector unit to compare performance gain and power increase. With the vector unit, this approach resulted in an average fourfold geometric performance gain with a modest average device-power increase of only 4.5%.

Low-power-code examples include general control or data-plane applications with significant packet throughput. Such applications involve many interrupts and conditional branches that branch-prediction hardware cannot accurately predict. Furthermore, these applications also tend to have fewer situations in which you can advantageously use execution-unit parallelism.

In experiments on Freescale's PowerQuicc III processors to determine the relative power of applications, an IPv4 (Internet Protocol Version 4) forwarding application dissipated about 5 to 10% lower core power than a Dhrystone 2.1 benchmark.

QUIZZING CHIP VENDORS ON POWER

With tight constraints on supply power, limited board space, height restrictions for heat sinks due to the presence of adjacent boards, and physical limits to cooling using forced-air convection in today's designs, system designers must carefully assess power requirements when selecting processors. Simply using a power number from a product brief when selecting a processor can result in surprises later when you attempt the actual hardware design and layout.

The following questions are useful references for helping chip vendors clarify their power specifications beyond the minimal footnotes in their hardware specifications and helping designers more accurately compare specifications among vendors:

Can you use the typical power for thermal design?
In most cases, it is likely that the thermal-design power needs to be higher than the typical power. Even if the vendor deems a power number suitable for thermal design with a processor, the following questions further probe this issue to ensure that the vendor's claims are accurate.

Does the vendor base the specified power on case temperature or on junction temperature?
When comparing processors, it is best to compare power at identical junction temperatures. This process involves some arithmetic to convert a case temperature to a junction temperature using the junction-to-case thermal resistance. Also, you may have to extrapolate the power number to a junction temperature to make a fair comparison. The vendor should be able to provide guidance on the power at different junction temperatures.

Does the vendor measure the power at the nominal or at a slightly lower voltage?
Careful inspection of the hardware specification is necessary to ensure that the vendor is quoting the power at the nominal operating voltage, not at a slightly lower voltage, to provide a more attractive number.

Is the application the vendor uses to determine typical power conservative or closer to a best-case scenario?
A maximum-packet-throughput scenario does not necessarily correspond to worst-case power dissipation. Dhrystone does not perform any I/O operations but dissipates higher power than I/O-intensive applications. Interrupts in an I/O-intensive application can cause significant numbers of pipeline stalls, such that power is lower than in a cache-resident application running in tight loops. Designers should ensure that the scenario represents the worst case in their applications before using the typical-power number for thermal-design purposes.

Is the typical-power number applicable to 100% of production parts?
Parts from a typical process generally have average static power, and worst-case process parts dissipate maximum static power. Some vendors provide typical power numbers based on a typical process, rather than a worst-case process. Therefore, production parts may exceed the specified typical-power value under the given conditions. For thermal design, typical-power values for worst-case processes are necessary as guidelines. Also, when profiling the power of an application using a development system or in a prototype, you may need the vendor's help to validate whether the power measurements correspond to a typical process or a worst-case process. You can also use a device from a worst-case-process corner with the highest possible static power in the prototype for power measurements.

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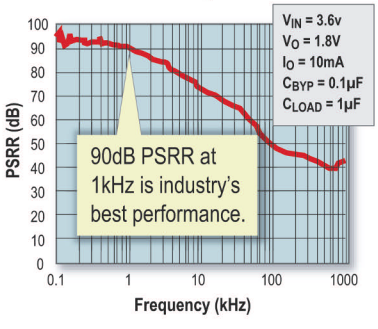


Shhhhhhh... We're Trying to Focus Here

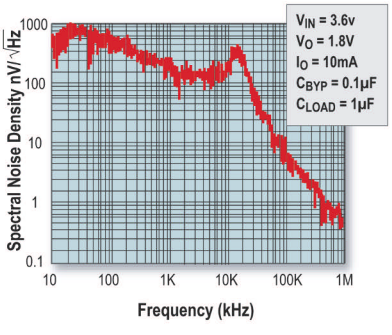
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ISL9000	90dB	30µ	300	300	42	1.8%
ISL9007	75dB	30µ	400	-	50	1.8%
ISL9011	70dB	30µ	150	300	45	1.8%
ISL9012	70dB	30µ	150	300	45	1.8%
ISL9014	70dB	30µ	300	300	45	1.8%

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This result was initially surprising, given that the Dhrystone code and data reside completely in Level 1 cache and do not involve any I/O. In contrast, the IPv4 application involved heavy use of the Ethernet interfaces, the DDR interface, internal DMA engines, and the Level 2 cache for header stashing. The lower core power in the IPv4 application was due to interrupts related to reception and the transmission of packets, which caused pipeline stalls. Dhrystone had no interrupts, and most of the branches were predictable; hence, fewer pipeline stalls occurred. Note that I/O power was higher in the IPv4 application than in Dhrystone.

On-chip I/O power can be considerable for some high-speed I/O interfaces, such as DDR, RapidIO, and PCI Express. Such high-speed interfaces can each easily dissipate more than 0.5W. Analogous to core power, the I/O power an interface dissipates depends on the frequency, voltage, temperature, number of pins, and the usage level of the interface. You can express the power dissipated on an I/O pin as $P=P_0+ACV^2F$, where A is the activity level of the pin, C is its capacitive loading, V is the interface voltage, F is the clock frequency of the interface, and P_0 is the static-power component.

DHRYSTONE BENCHMARKS

The Dhrystone benchmark also falls into the category of high-power code because both the code and the data sections fit comfortably within Level 1 caches in today's high-end processors. Although Dhrystone generally does not represent real applications as a performance measure, it can be a useful gauge for estimating power dissipation. In comparisons with a large set of EEMBC benchmarks, Dhrystone's power dissipation was within 2% of that of EEMBC benchmarks on several Freescale PowerPC processors. Note that EEMBC benchmarks mimic critical portions of real applications. In reality, EEMBC benchmarks exercise only the core and memory interfaces, so the similarity in power to Dhrystone is not too surprising.

Besides being freely available, Dhrystone code also fits into a production tester, making Dhrystone convenient as a test vector for characterizing power dissipation. Experiments on Freescale's PowerQuicc III devices show that Dhrystone dissipates more power than an IPv4 forwarding application. Hence, Dhrystone provides a suitable upper bound for many realistic applications, and you can use it for characterizing typical power.

Although the use of Dhrystone for characterizing typical power may work well for some integrated processors, its suitability for any given integrated communication processor depends on the processor-core power relative to other blocks within the system.

MAXIMUM POWER

The power-supply design of a processor requires maximum power-dissipation information for each power rail. Designers should ensure that this data is available from the chip vendors.

For the core-power rail, the maximum-power value should be the sum of the worst-case static power and the worst-case dynamic power possible from the device. The worst-case dynamic power should be higher than that you obtain from just running Dhrystone and should include power dissipation due to simultaneous operation of various internal blocks.

For rails supplying I/O interfaces, you should take into account a worst-case realistic usage of the interfaces. Ideally, the vendor should provide the power dissipation on each interface separately for each speed, width, and other attribute that applies to the interface. In this way, a designer may add the power contribution of each interface corresponding to each I/O supply rail.

FEATURES TO LOOK FOR

The availability of low core voltages—preferably below 1.5V—is desirable, because it is one of the most significant factors that helps to reduce power as die sizes shrink with processor generations. Flexible clock multipliers between the core and the platform are useful for running an application at a frequency combination that provides adequate performance and minimizes power.

In some applications, such as printers, in which a processor remains idle until a job arrives, the availability of low-power modes is important to meet EnergyStar requirements. Multiple low-power modes may be available, and the specific low-power mode depends on application requirements. For instance, in PowerQuicc III, you can use the sleep mode to shut down the core and all I/O blocks; an external interrupt can awaken the device in this mode. For an application that needs to keep I/O blocks active to awaken the core when packets arrive, the nap mode is ideal, because it still saves significant power by stopping the core. In a multiprocessor application that must maintain cache coherency, the doze mode is suitable, because it permits you to snoop within the caches while the core is off.

Another important factor is the presence of dynamic power-management capability. With dynamic power management, gating clocks automatically minimize power consumption when a block is idle. This feature may be automatic or may require manual enablement, depending on the device. It generally has little or no performance impact and it conserves power; hence, you should use it when available.

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Dynamic management of I/O power is also important for minimizing the overall power consumption in applications. For instance, the DDR memory controller should be able to reduce power consumption by negating the SDRAM clock-enable signal when no transactions are pending to the SDRAM; the usual trade-off for enabling such a feature is a one-clock access-latency penalty.

Integrated parts come with an assortment of interfaces. However, a given application may not use some of the interfaces or internal blocks. Therefore, it is important to be able to shut down any unused blocks to save power. Furthermore, you may also reduce the power estimates that the vendor provides by the amount such unused blocks save. EDN

AUTHOR BIOGRAPHY

Ravi Chandran is a system architect in Freescale Semiconductor's networking and computing-systems group (Austin, TX). His responsibilities include determining product and system requirements and strategy, tracking industry standards, and benchmarking. He has a bachelor's degree in electrical engineering from the University of Michigan (Ann Arbor) and a master's degree in electrical engineering from the University of Notre Dame (Notre Dame, IN).

Intersil Battery Charger ICs

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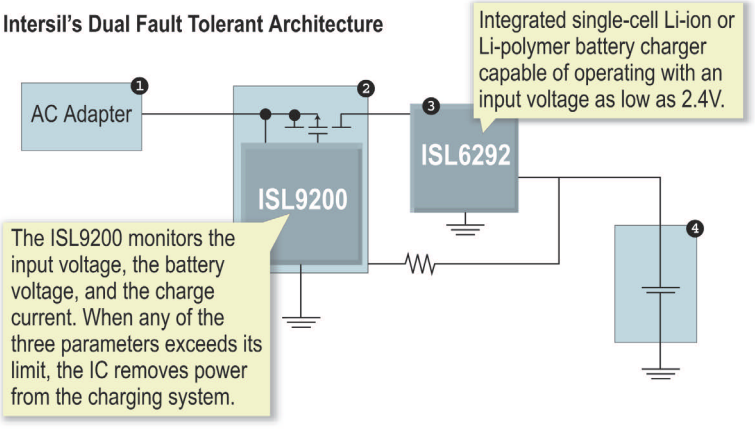


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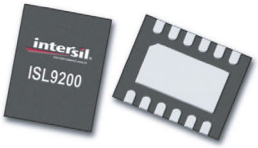
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Dual-Fault FMEA (Failure Mode and Effects Analysis)

POTENTIAL FAILURES				Consequence of Dual Failure
❶	❷	❸	❹	
●	●			❸ will fail but the protection module in the battery pack will protect the battery cell.
●		●		Both ❷ and ❹ will protect the battery cell.
●			●	❸ will limit the battery voltage. ❷ has an additional level of protection.
	●	●		The protection module in the battery pack protects the cell.
	●		●	❸ will limit the battery voltage to 4.2V, within 1% error.
		●	●	❷ will sense an over voltage case and remove the power from the system.



- User programmable overcurrent protection threshold
- Input overvoltage protection in less than 1µs
- Battery overvaltage protection
- High immunity of false triggering under transcients
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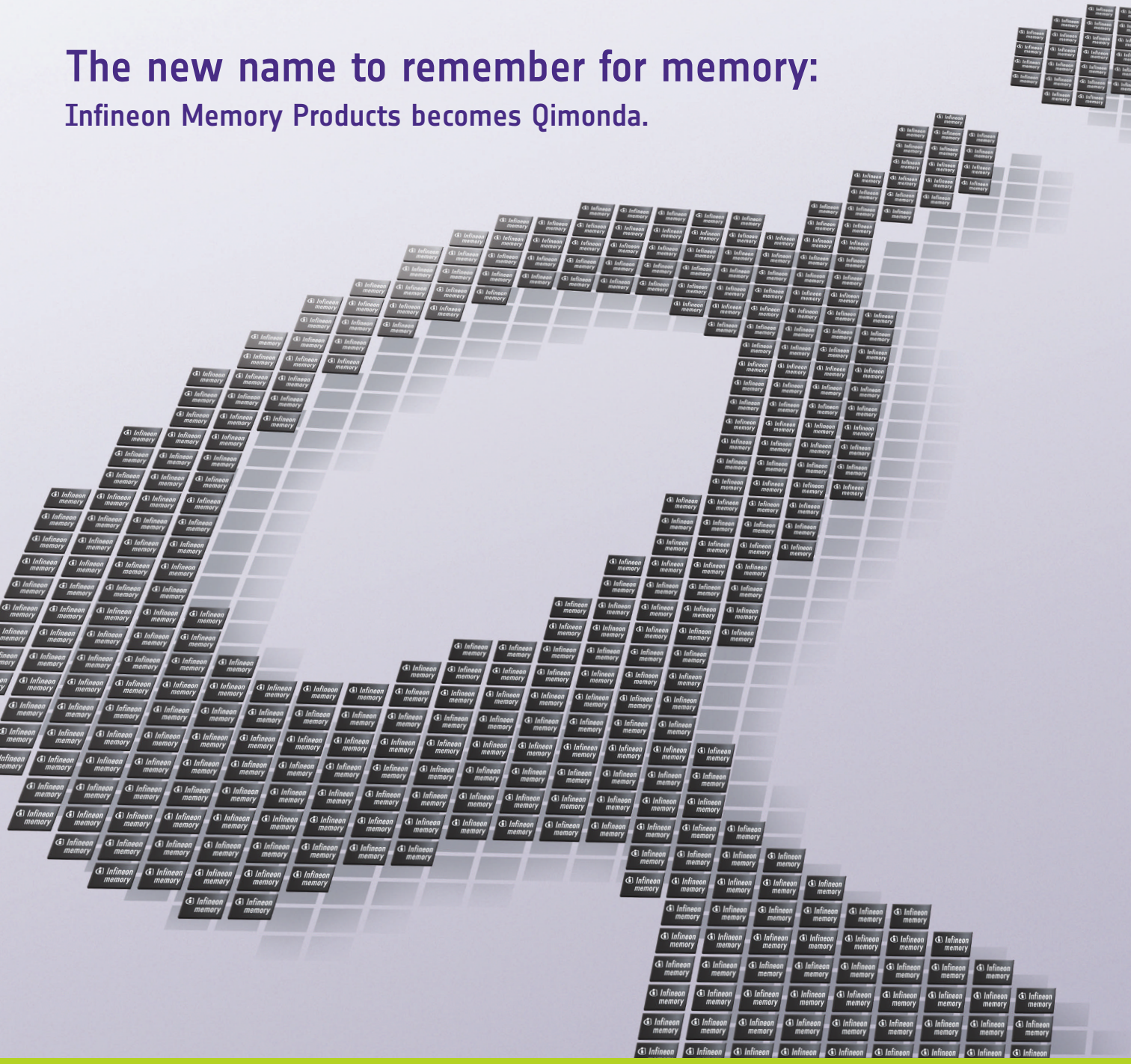
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TEXAS INSTRUMENTS

POWER MANAGEMENT

Analog Applications Journal

BRIEF

IC Powers Portable Photographic Flash

By Scot Lester • Portable Power DC/DC Applications

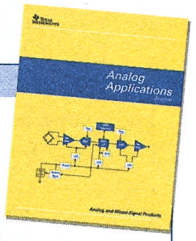
Introduction

Upper end photographic equipment, either optical film- or digital-based, requires Xenon flash tubes in order to photograph in low-light conditions. Xenon flash tubes can provide a burst of high-intensity light that is essential for photography of objects at a distance, moving at high speeds, or in low-light conditions. The light spectrum generated by a Xenon gas discharge tube closely replicates that of the sun, therefore providing very accurate color reproduction.

Xenon flash tubes require a high voltage across their electrodes in order to flash once a trigger signal is applied. This voltage is typically around 300 volts. All of the energy needed to flash the lamp is stored in a bulk capacitor called a photoflash capacitor. Once the lamp is triggered, all of the energy stored in the photoflash capacitor is discharged through the flash tube to produce light. The stored energy in the photoflash capacitor is provided by a specialized boost converter that charges the photoflash capacitor up to 300 V from a much lower battery input voltage. In the past, this converter was built of bulky discrete components that were difficult to incorporate into the space available in small devices such as a camera.

Texas Instruments' TPS65552A photoflash charger IC is a highly integrated photoflash charger that greatly simplifies and reduces the size of the photoflash charger circuit. Figure 1 shows a photoflash capacitor charger based on this device. The TPS65552A provides all the necessary charging controls, output feedback, charge completion status, IGBT gate driver and circuit protections necessary to implement a small, efficient photoflash charger.

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The TPS65552A is based on a flyback topology. The output voltage is sensed during the off period of the internal switch, at which time the output voltage is reflected back to the input through the transformer. This eliminates the need for a bulky, high-voltage feedback network on the output and also provides electrical isolation from the input to the output. Once the output voltage reaches its target value, the TPS65552A will automatically stop charging and an open collector output goes low, thus signaling a 'ready to flash' condition. This output can drive a status-indicating LED or an input to a microcontroller.

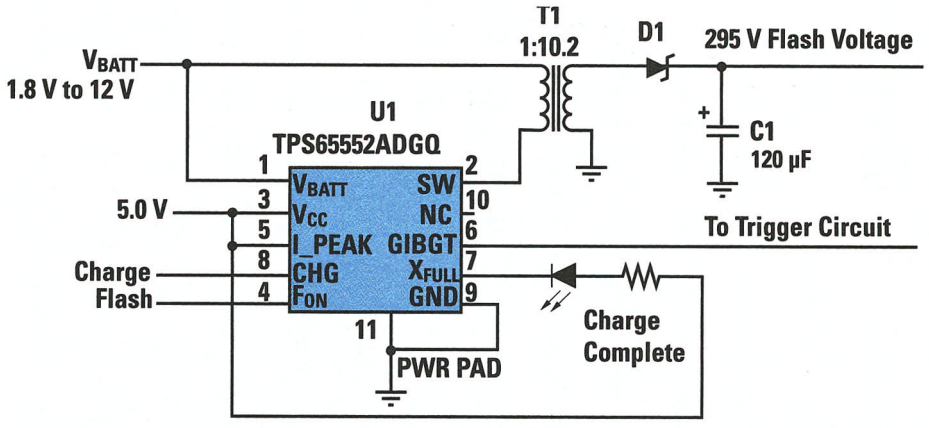


Figure 1 – TPS65552A photoflash charger

The I_PEAK pin of the TPS65552A controls the peak current that flows through the primary of the flyback transformer, T1, during each switch cycle. To adjust the capacitor charging time, the primary current can be dynamically adjusted from 0.9 amps to 1.8 amps by changing the voltage applied to the I_PEAK pin. This feature allows a microcontroller to dynamically control the current draw

The TPS65552A has an integrated high-current buffer to drive the gate of an IGBT used in the trigger circuit. The IGBT can be driven on and off during flashes to support functions such as red-eye reduction or Evaluated Through The Lens (E-TTL) flash modes.

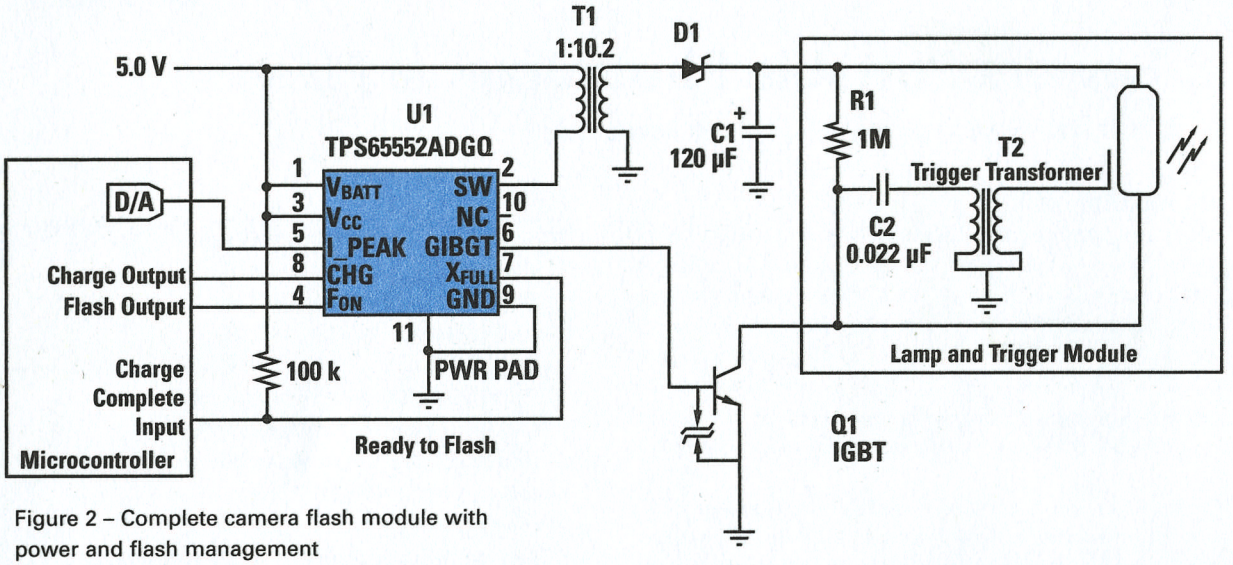


Figure 2 – Complete camera flash module with power and flash management

of the charger for power management. For example, in a digital still camera, a microcontroller can reduce the charger current when a high-current zoom motor is operating so that both can function at the same time and not exceed the maximum current capability of the camera's battery. This feature can also be used to extend battery run time. Reducing the peak currents during charging reduces the average current consumption so that a weak battery, with diminished current capability, can still charge the photoflash capacitor.

Historically, the flash has been triggered with a pushbutton switch or a Silicon-Controlled Rectifier (SCR). However, newer flash modes such as red-eye reduction use multiple bursts of the Xenon lamp. The lamp is triggered for a short flash that does not fully discharge the photoflash capacitor. Then, after a short delay, the lamp is retriggered for the main flash. The pushbutton and SCR cannot reliably start and stop the lamp mid-flash. The Insulated Gate Bipolar Transistor (IGBT) is capable of handling the currents, which are typically 150 amps during a flash. However, like a MOSFET, the gate of the IGBT requires a large current pulse in order to quickly turn on. Therefore, a high-current driver is required to drive the gate of the IGBT.

Device	RefDes	Description	MFR
330 FW 120A	C1	Capacitor, Aluminum, 120-uF, 330-VDC, ±20%	Rubycon
C3216X7R2J223KT	C2	Capacitor, Ceramic, 0.022-uF, 630-V, X7R, 10%	TDK
ES1G	D1	Diode, Rectifier, 1-A, 400-V	Diodes Inc.
36FT050	FL1	Flash Tube, 400v Max	Xicon
SSM25G45EM	Q1	Trans, NChan Insulated-Gate Bipolar, 450V, 150A	Silicon Standard
CTX16-17360	T1	Transformer, Flyback, 1:10.2	Coiltronics
422-2304	T2	Transformer, Trigger	Xicon

Reference:

1. TPS65552 Datasheet (SLVS567)

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BY STEPHEN MEEK • ON SEMICONDUCTOR

Maintain thermal stability for power-MOS devices

POWER MOSFETs CAN EXPERIENCE DESTRUCTIVE THERMAL EFFECTS AT RELATIVELY LOW DRAIN VOLTAGES AND CURRENTS THAT ARE WELL WITHIN TRADITIONAL, SAFE BOUNDARIES. HOWEVER, DESIGNERS CAN USE BASIC SPICE-MODEL PARAMETERS TO PREVENT THERMAL INSTABILITY IN THESE DEVICES.

Power MOSFETs can experience destructive thermal effects at relatively low drain voltages and currents that are well within the traditional SOA (safe-operating-area) boundaries. For typical SOA curves, in which gate-to-source voltage is larger than the threshold voltage, the increasing on-resistance of the MOS device dominates and effectively limits thermal runaway. Destructive failure can result, however, if the device is biased at a low gate-to-source voltage, such that sensitivity to the decreasing threshold voltage overwhelms the increasing channel resistance as temperature rises. You can use basic Spice-model parameters to estimate the minimum gate drive to prevent thermal instability and resultant damage to the device.

MOSFETs IN THE SATURATION REGION

For a MOSFET in the saturation region,

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2, \quad (1)$$

where I_D is drain current, μ is electron mobility, V_T is the threshold voltage, V_{GS} is the gate-to-source voltage, C_{OX} is the oxide capacitance, W is the gate width, and L is the gate length. Electron mobility and threshold voltage are the significant temperature-dependent terms.

The threshold of thermal stability occurs at the $V_{GS}-V_T$ value, where the rate of change of drain current with temperature is zero:

$$\frac{\partial I_D}{\partial T} = \frac{\partial \mu}{\partial T}\times\left\{\frac{C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2\right\} - \frac{\partial V_T}{\partial T}\times\left\{\mu C_{OX}\frac{W}{L}(V_{GS}-V_T)\right\}. \quad (2)$$

Substituting for I_D,

$$\frac{\partial I_D}{\partial T} = \frac{\partial \mu}{\partial T}\times\left\{\frac{I_D}{\mu}\right\} - \frac{\partial V_T}{\partial T}\times\left\{\frac{2I_D}{(V_{GS}-V_T)}\right\} = I_D\times\left\{\frac{1}{\mu}\frac{\partial \mu}{\partial T} - \frac{2}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}\right\}. \quad (3)$$

Recognizing that both $\partial\mu/\partial T$ and $\partial V_T/\partial T$ are negative, **Equation 2** shows that drain current increases or decreases with temperature, depending on the magnitude of $V_{GS}-V_T$. Setting this rate of change to zero gives $V_{GS}-V_T$ at the threshold of stability:

$$\frac{1}{\mu}\frac{\partial \mu}{\partial T} = \frac{2}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}, \quad (4)$$

or

$$V_{GS}-V_T = 2\mu\times\frac{\partial V_T/\partial T}{\partial \mu/\partial T}. \quad (5)$$

$V_{GS}-V_T$ must be greater than the value in **Equation 5** to ensure thermal stability, $-\partial I_D/\partial T$. Note that the rate of change with temperature is proportional to I_D, but the threshold of thermal stability depends only on mobility and the temperature coefficients of mobility and threshold voltage. You can derive the mobility value for a typical MOS power device, the NTD60N02, from the Spice-model-file parameter for K′ on the manufacturer's Web site: $K' = \mu\times C_{OX}$, and $C_{OX} = \epsilon_{OX}/t_{OX}$. With $K' = 18.1\ \mu A/V^2$ from the model file, permittivity that standard texts define, and an oxide thickness of 400 angstroms, mobility is $\mu = 206(cm^2/V\times sec)$ for this process. Mobility varies with temperature in a manner proportional to T^{-n}, where n is typically about 1.5 (**Reference 1**). You determine an expression for mobility as a function of temperature by setting $206 = C\times T^{-1.5} = C\times 300^{-1.5}$ at room temperature, where T = 300K). This calculation equates to a proportionality constant of $C = (206/300^{-1.5}) = 2.86\times 10^6$. The rate of change of mobility with temperature (**Reference 2**) for this case is then:

$$\frac{\partial \mu}{\partial T} = -N\times C\times T^{-N-1} = -1.5\times(1.1\times 10^6)\times 300^{-2.5} = -1.06\frac{CM^2/V\times sec}{°K}. \quad (6)$$

Typical values for threshold-voltage variation with temperature are in the range of $(\partial VT/\partial T) = -2[(mV)/°K]$. Using these values of mobility and temperature variation:

$$V_{GS}-V_T = 2\times 550\times\left(\frac{-0.002}{-2.75}\right) = 0.8V \quad (7)$$

for a MOS device with the mobility [$550(cm^2/V\times sec]$ operating in the saturated region. You can then add the Spice-model value for V_T to the above result to determine the minimum gate-

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to-source voltage necessary for thermal stability.

MOSFETs IN THE LINEAR REGION

You can apply the same analysis to the drain-current expression for a MOS device in the linear region of operation:

$$I_D = \mu C_{OX} \frac{W}{L}\left\{(V_{GS}-V_T)\times\left(V_{DS}-\frac{V_{DS}^2}{2}\right)\right\}, \quad (8)$$

where the V_{DS}^2 term is small enough for you to ignore in **Equation 9**:

$$\frac{\partial I_D}{\partial T} = \frac{\partial \mu}{\partial T}\times\left\{C_{OX}\frac{W}{L}(V_{GS}-V_T)\times V_{DS}\right\} - \frac{\partial V_T}{\partial T}\times \left\{\mu C_{OX}\frac{W}{L}V_{DS}\right\} = \frac{\partial \mu}{\partial T}\times\left\{\frac{I_D}{\mu}\right\} - \frac{\partial V_T}{\partial T}\times\left\{\frac{I_D}{(V_{GS}-V_T)}\right\} = I_D\times\left\{\frac{1}{\mu}\frac{\partial \mu}{\partial T} - \frac{1}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}\right\}. \quad (9)$$

Again, the drain-current rate of change with temperature shows that drain current increases or decreases with temperature, depending on the magnitude of $V_{GS}-V_T$. Setting this rate of change to zero yields **Equation 10** or **11**:

$$\frac{1}{\mu}\frac{\partial \mu}{\partial T} = \frac{1}{(V_{GS}-V_T)}\frac{\partial V_T}{\partial T}, \quad (10)$$

or

$$V_{GS}-V_T = \mu\times\frac{\partial V_T/\partial T}{\partial \mu/\partial T}, \quad (11)$$

which differ from the expression for a device in saturation, **equations 4** and **5**, by a factor of two. Thus, for the same device-channel mobility of 550($cm^2/V\times sec$), the minimum gate drive to maintain thermal stability in the linear region is half that in saturation, or $V_{GS}-V_T=0.4V$.

You can find Spice models for many discrete power MOSFETs on the manufacturers' Web sites. These models are usually more basic than the BSIM3 models designers commonly use for IC simulation, so the U0 value for mobility may default to the value of 600($cm^2/V\times sec$), which Spice simulator references use (**Reference 3**).EDN

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Steve Meek is an analog-design engineer at On Semiconductor (Phoenix), where he is responsible for the design and development of power-management ICs. He has a master's degree in electrical engineering from Montana State University (Bozeman, MT). His personal interests include audio electronics, mountaineering, and reading.

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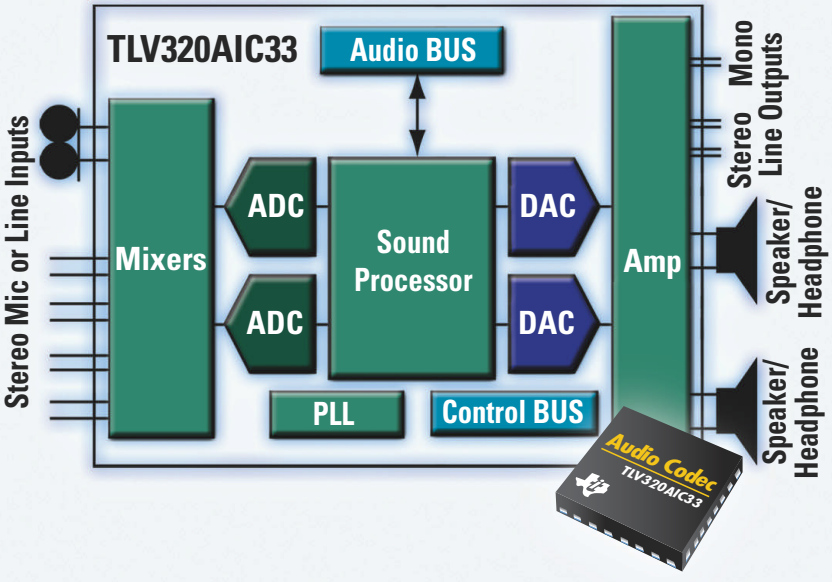
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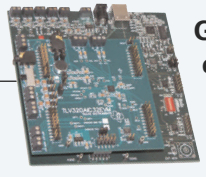
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BY BARRY L DORR • DORR ENGINEERING

A simple software lowpass filter suits embedded-system applications

BUILDING A DIGITAL EQUIVALENT OF AN ANALOG LOWPASS RC FILTER REQUIRES JUST A COUPLE OF LINES OF FIXED-POINT C CODE.

Hardware-design engineers have long recognized the usefulness of RC lowpass filters (**Figure 1**). Lowpass filters are useful for performing signal conditioning, removing noise from a signal, or rejecting unwanted signals. The first-order recursive filter is the digital equivalent of the RC filter, and, as the ratio of the sample frequency to the bandwidth increases, their responses become identical.

All lowpass filters produce a weighted average of the current input value and past inputs. A filter's characteristics depend on the weighting used for the past inputs. For example, a lowpass filter (**Figure 2**) smoothes noisy input signals. One possibility for weighting the past-input samples is to give them equal weight. Although this approach produces a useful lowpass filter, it makes more intuitive sense to weigh newer samples more heavily than older samples.

A designer can use recursion to implement a weighting function (**Figure 3**). This approach minimizes the processing impact of the multiplications in this filter because the designer can implement the multiplications as left or rights shifts in the software. The designer feeds data samples with bit width B1 into the filter at a fixed sample rate. Bit width B2 may be larger than bit width B1. The summing block adds the input sample to the last output sample, and the delay is a digital delay of one sample. The parameter k is a shift value that controls the filter bandwidth. Mathematically, the recursion in **Figure 3** is: $y(n)=(1-2^{-k})\times y(n-1)+x(n)$, where x is the input, y is the output, and n is the sample index.

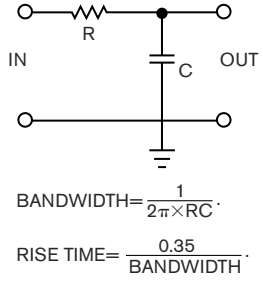


Figure 1 Lowpass filters are useful for performing signal conditioning, removing noise from a signal, or rejecting unwanted signals.

As an example of filter operation, suppose that $k=4$ so $1-2^{-k}=0.9375$, the value at the delay output is zero, and the filter input is a single sample of one followed by all zeros. If you use the summing block as the output, the first output from the filter is one. When you feed this output back to the summing block, the multiplier scales it, and it becomes 0.9375. The next output is 0.9375^2 or 0.8789, and the nth output is 0.9375^n. This sequence is the impulse response of the filter, but it is also the weighting function (**Figure 4**). Good stuff is going on here for those who like math, but we'll stick to the implementation.

SPECIFYING THE FILTER RESPONSE

A designer can specify the filter response in either the frequency domain or the time domain. Which one to use depends on the type of problem you are working on. If noise or unwanted tones are the problems, then the frequency-domain specification or bandwidth is appropriate. To reject impulse-noise hits, or smooth measured data, the time-domain specification or rise time may work better.

When working in the frequency domain, the designer specifies the 3-dB frequency or bandwidth of the filter. At this frequency, the amplitude of the output drops to 0.707 times the amplitude that a dc signal causes (**Figure 5a**). You can estimate the atten-

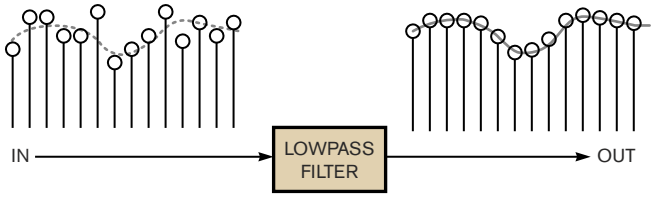


Figure 2 A filter's characteristics depend on the weighting used for the past inputs. For example, a filter smoothes noisy input signals.

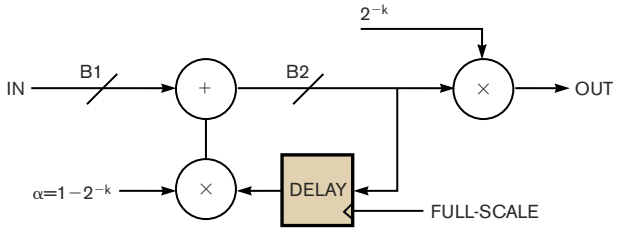


Figure 3 A designer can use recursion to implement a weighting function.

uation at higher frequencies because doubling the frequency approximately halves the amplitude. **Table 1**, which is normalized to a sample rate of 1 Hz, shows the normalized bandwidth and rise time for several values of k. To get the actual bandwidth, multiply the value in the **table** by the sampling frequency.

When working in the time domain, the designer specifies the rise time of the output in response to a step input. **Figure 5b** shows the filter output when the input changes from all zeros to all ones, which causes the output to gradually move from zero to one. The rise time is the time necessary for the filter output to move from 10 to 90% of the final value. **Table 1** specifies the rise time in number of samples.

Before writing code to implement this filter, the designer must specify the number of bits necessary for the summing block and the delay. Because the filter is basically an averaging device, the range of the summing-block output is larger than the range of the input signal if there is to be no loss in precision. Fortunately, it is easy to predict the growth in the output-register width because the dc gain from the input to the summing-block output is 2^k, so bit width B2 from **Figure 2** is k bits wider than bit width B1. You can maintain a unity gain by multiplying the summing-block output by 2^{-k}.

The fixed-point code in **Listing 1** implements a filter for the case of k=4. Using a power of two for k enables the use of right shifts in the code to avoid the performance hit from the multiplier blocks. Using a 32-bit integer for the summing block and delay accommodates the four bits of growth in the output register. When using this code, make sure that your compiler sign extends when right-shifting a signed number.

The first-order recursive filter, or "leaky integrator," is a simple yet powerful filter that is a time-tested approach for many filtering applications, and this implementation requires no multiply instructions. The steps to quickly and accurately implement this filter are to specify the filter using either the rise time or the bandwidth, allocate k additional bits for the summing block and delay to accommodate register growth, and implement the filter by substituting shifts instead of multiply instructions as the example code shows. EDN

TABLE 1 NORMALIZED BANDWIDTH AND RISE TIME FOR VARIOUS VALUES OF k

k	Bandwidth (normalized to 1 Hz)	Rise time (samples)
1	0.1197	Three
2	0.0466	Eight
3	0.0217	16
4	0.0104	34
5	0.0051	69
6	0.0026	140
7	0.0012	280
8	0.0007	561

LISTING 1 CODE FOR THE SIMPLE FILTER

```
#define FILTER_SHIFT 4          // Parameter K
#define sint32 (signed long)    // Specify 32-bit integer
#define sint16 (signed short)   // Specify 16-bit integer

sint32 filter_reg;              // Delay element – 32 bits
sint16 filter_input;            // Filter input – 16 bits
sint16 filter_output;           // Filter output – 16 bits

// Update filter with current sample.
filter_reg = filter_reg - (filter_reg >> FILTER_SHIFT) + filter_input;

// Scale output for unity gain.
output = filter_reg >> FILTER_SHIFT;
```

AUTHOR'S BIOGRAPHY



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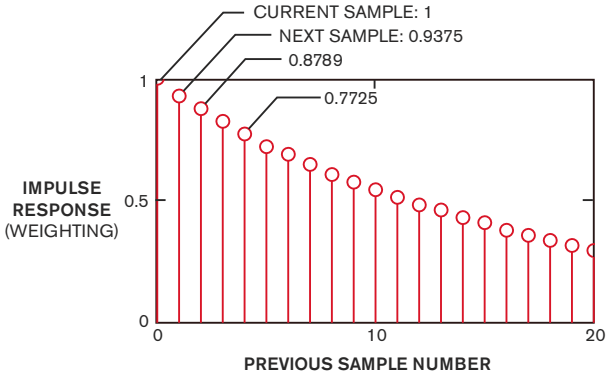


Figure 4 This sequence is the impulse response of the filter, but it is also the weighting function; k=4, so $1-2^{-k}=0.9375$.

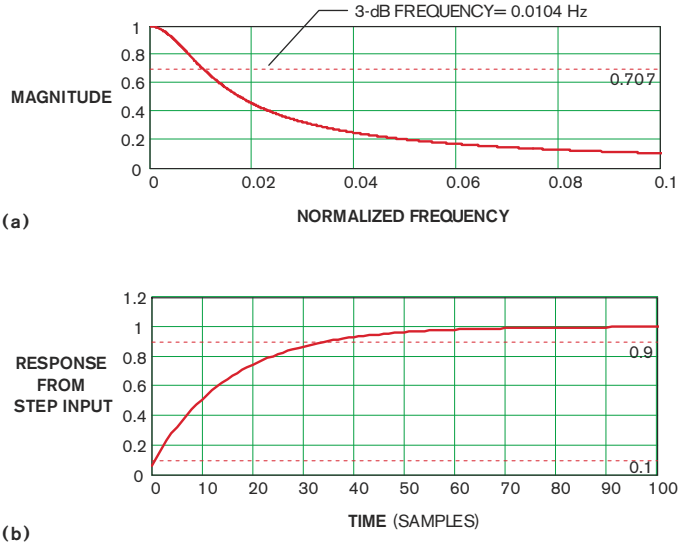


Figure 5 At this frequency, the amplitude of the output drops to 0.707 times the amplitude that a dc signal causes (a). When the input changes from all zeros to all ones, the output gradually moves from zero to one (b).

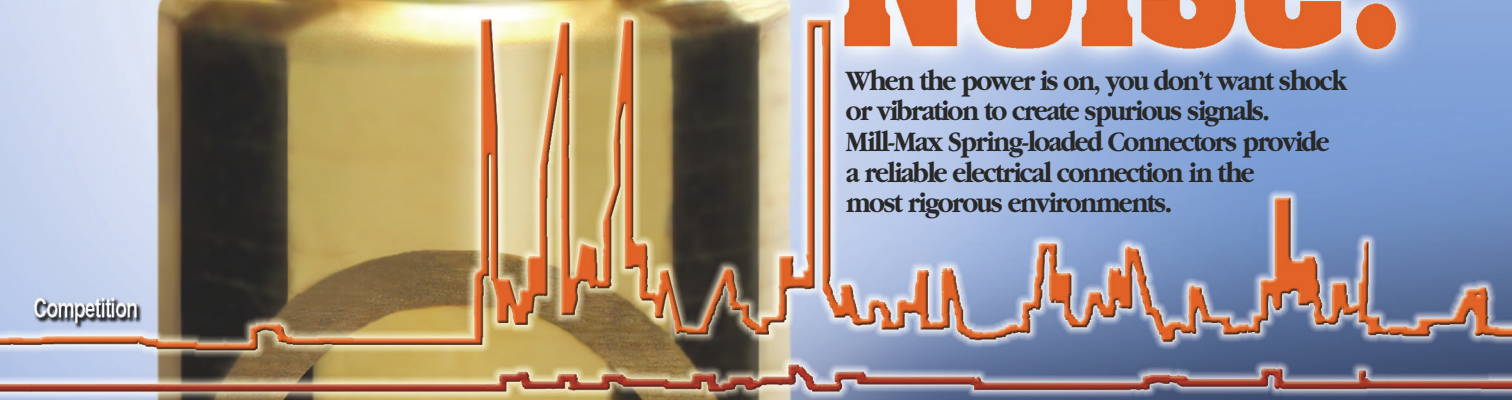
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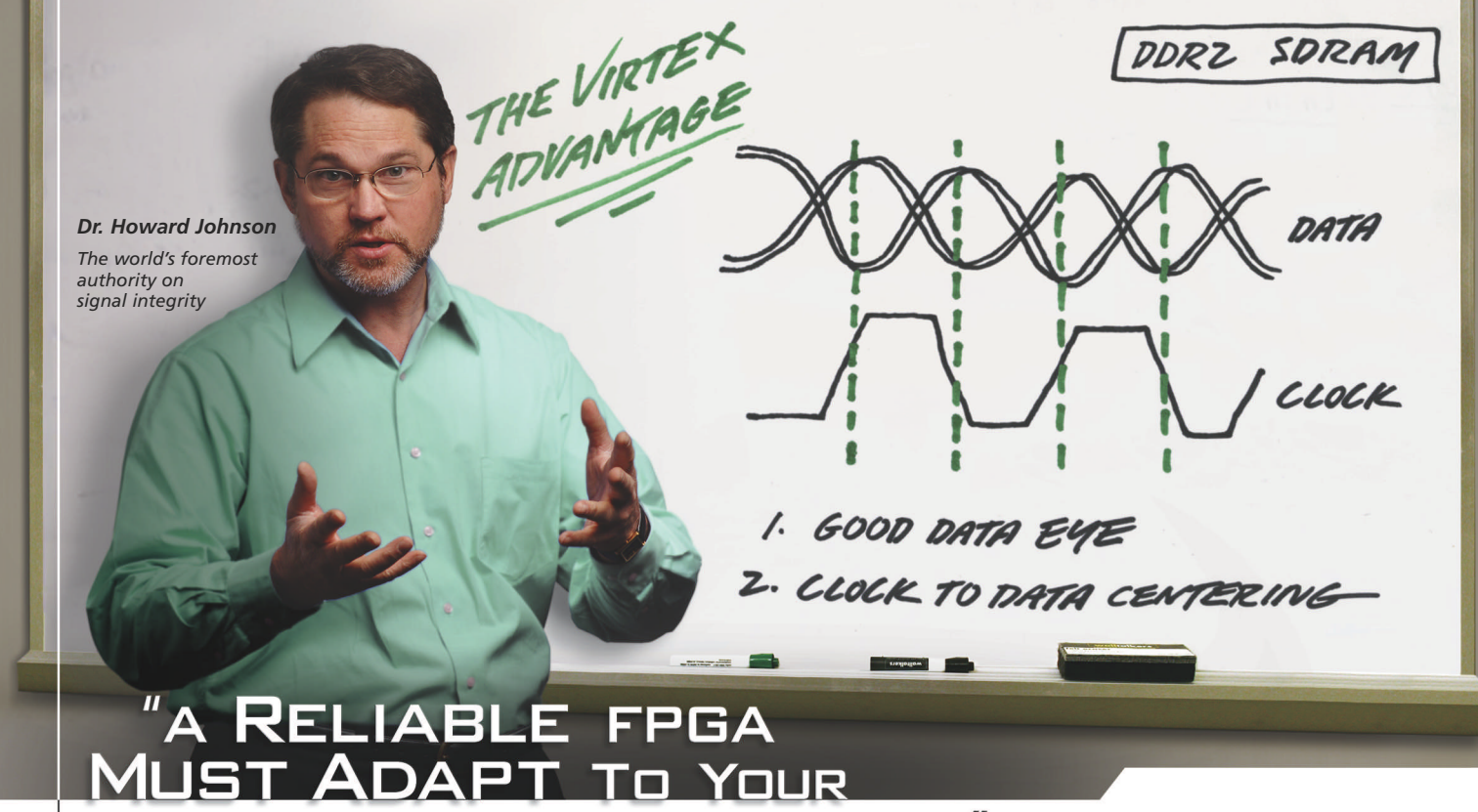


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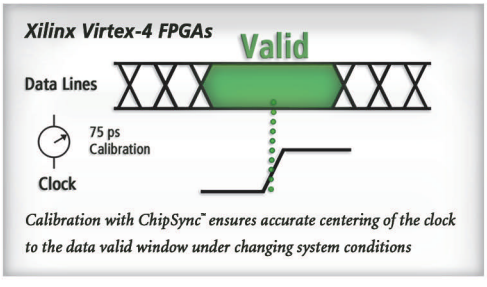
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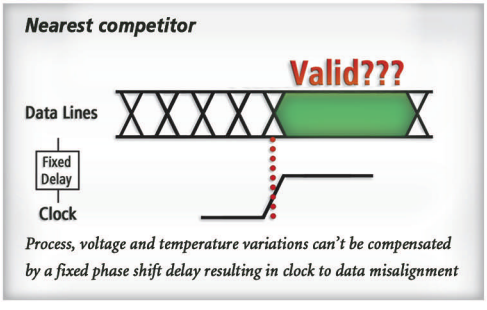
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BY GAURANG KAVAIYA • MICROCHIP TECHNOLOGY

Don't pay for level translators in systems using multiple power-supply voltages

BECAUSE LOWER-POWER-SUPPLY-VOLTAGE VERSIONS OF ICs BECOME AVAILABLE AT DIFFERENT TIMES, MANY OF TODAY'S SYSTEMS MUST USE SEVERAL VOLTAGES. EVEN SO, YOU CAN OFTEN AVOID THE EXPENSE OF LEVEL TRANSLATORS.

From its early days, the semiconductor industry's mantra has been smaller, better, faster, and cheaper. Today's handheld computing devices are more powerful than the first computers, which required separate buildings. Manufacturers have so far achieved the simultaneous dramatic improvements in cost, performance, and speed by reducing the size of the individual transistors that make up semiconductor devices. This size reduction has had an interesting consequence. As transistors shrink, their operating voltage also shrinks. The most popular power-supply voltage in embedded systems used to be 5V. Now, though, most components in typical embedded systems are moving toward lower supply voltages to take advantage of the industry's newest trends. On the other hand, some system components take longer than others to evolve. Therefore, during the transition to lower voltage, components of a system often require different supply voltages. This situation creates challenges for embedded-system designers. One approach is to use level translators, although they can be costly. This article discusses some low-cost ways to interface a 3.3V microcontroller to a 5V peripheral.

If you are moving your 5V design to 3.3V, the first things to look for are 3.3V versions of the 5V devices. In most cases, you'll find equivalent devices that operate from 3.3V. Usually, 3.3V devices are available at the same—or lower—cost. If you can't find an alternative device that runs at 3.3V, you may need to use two supply voltages. This article's main focus is on designs that use two supply-voltage rails (**Figure 1**).

When you bring together people from different parts of the world, you need to ensure that they can communicate with each other. The same is true when you bring together the 5 and 3V worlds. You must first understand the logic-voltage levels and input/output structure. For inputs, you need to consider high and low input voltage. When you interface a 3.3V system with a 5V device, high input voltage tends to be a bigger problem than low input voltage. Still, you can't ignore the low-input-voltage spec. To ensure proper logic detection, the driving device must produce an output voltage higher than the receiving device's minimum-high-input-voltage spec. However, voltages that are too high aren't good, either.

Almost all CMOS devices have some kind of ESD (electrostatic-discharge) protection on all I/O pins. The most common implementation of this protection uses clamping diodes from the I/O pins to V_{DD} and V_{SS}. Generally, this arrangement translates into a maximum input-voltage spec of $V_{DD}+0.3V$ and a minimum voltage spec of $V_{SS}-0.3V$. If you exceed these specs, the protection diodes may start conducting. If the input terminal has no series resistor, the result can be very high current through these diodes, potentially causing latch-up. You don't want to cre-

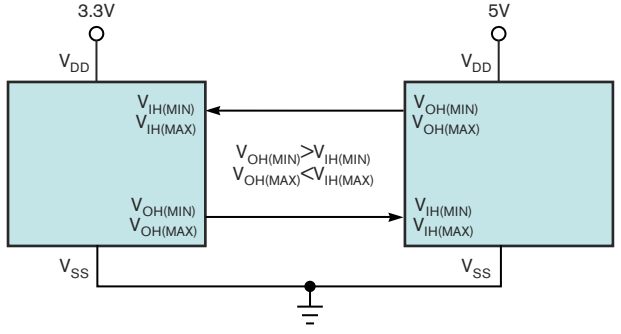


Figure 1 In a two-rail system, devices with different logic levels must communicate.

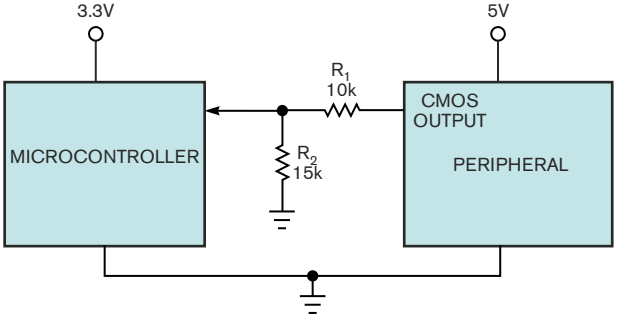


Figure 2 A resistive divider brings a 5V signal in range for a 3.3V input.

ate this condition. If the voltage is high enough—that is, a 5V input in a 3.3V system—you need high series resistance to reduce the clamp current to a safe value. Also, if the resistance is large enough, the low pin and pc-board capacitances may be significant. That is, the RC time constant can cause signal delay. Many manufacturers recommend against the use of ESD-protection diodes for signal clamping. Therefore, a series resistor isn't the best option for feeding a 5V signal to a 3.3V device.

If you look at the logic levels of standard CMOS devices, most of them tend to have minimum high-input voltage of 0.7 or $0.8V_{DD}$. Maximum low-input voltage tends to be around 0.2 or $0.3V_{DD}$. For 5V logic, these levels translate into a high-input voltage of 3.5 or 4V and a maximum low-input voltage of 1 or 1.5V. At lower load currents, most CMOS devices produce output voltages close to the rail with a 0.1 or 0.2V drop. As the load current increases, high output voltage tends to be lower. In this scenario, you must consider the load current to determine the high output voltage.

RESISTIVE DIVIDER

Compared with a resistor in series with the input, a better option is to use a resistive divider to reduce 5V signals to a range suitable for 3.3V inputs (**Figure 2**). Select the resistor values to account for all tolerances. The following formulas assist in the calculation: With the 5V supply at its minimum value, $(R_2/(R_1+R_2))\times V_{OH(MIN)}>V_{IH(MIN)}$. With the 5V supply at its maximum value, $(R_2/(R_1+R_2))\times V_{OH(MAX)}<V_{IH(MAX)}$. You should also consider resistor tolerances in these calculations.

TTL-INPUT DEVICES

A simpler approach is to use a 5V device with TTL inputs (**Figure 3**). The minimum high-input voltage for a TTL device is 2.1V at drain-to-drain voltage of 5V. Most 3.3V devices can provide a much higher high-output-voltage level, even at high load currents. In this case, swap the peripheral for an equivalent device that has TTL-compatible inputs. If you search carefully, you should be able to find a similar device with TTL inputs. **Table 1** lists some examples. If you are using a standard digital-logic family that must run at 5V, you can find equivalent devices that have TTL inputs. For example, instead of the 74HC family, you can use the 74HCT family. If you need a level translator, use an HCT or a VHCT type of digital buffer. In most situations, this TTL-input-buffer approach is less expensive than the use of dedicated level translators.

DIODE CREATES 0.6V POSITIVE SHIFT

The output high-voltage level of a device operating at 3.3V is slightly lower than the input high-voltage, 0.7V at 3.5V, of a CMOS device operating at 5V. One simple way around this problem is to use a diode to provide the required voltage shift.

The circuit in **Figure 4** shifts the output by approximately 0.6V in the positive direction. Shifting this voltage by 0.6V brings it in range for a 5V CMOS input. The same amount of shift applies to the logic-low signal. Maximum low-voltage input

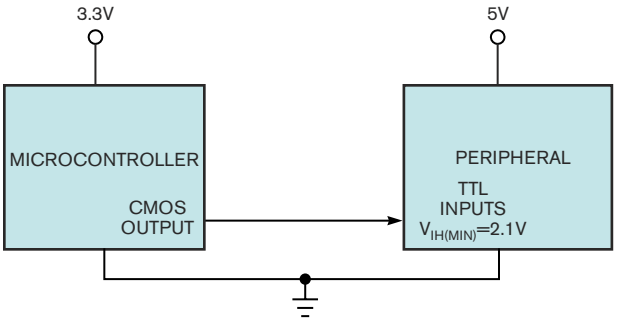


Figure 3 A 5V CMOS device can directly drive TTL inputs.

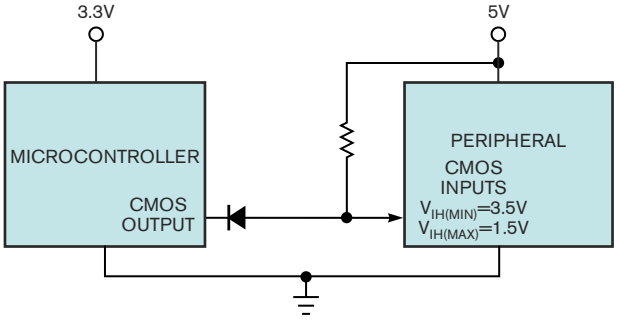


Figure 4 A diode and a resistor bring a 3.3V device output in range for a 5V input.

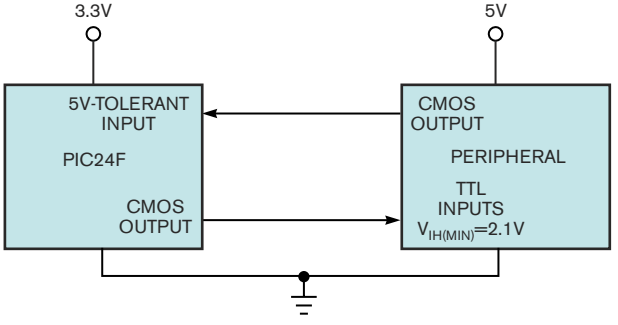


Figure 5 This simple interface works with 5V devices that have CMOS inputs.

for the CMOS is approximately 1.5V, so the shifted signal does not violate the input low-voltage spec. You need to consider a few things regarding this configuration, though. When the 3.3V device produces a logic-zero level, it increases the current the device draws from the power supply. You should also look at the 3.3V device's low-output-voltage spec at this current. Typically, the higher the sink current, the higher the input low voltage. In this case, you must take care to avoid violating the input-low-voltage spec. If the CMOS low-output voltage is higher, you

TABLE 1 DEVICES WITH CMOS INPUTS AND TTL-INPUT-EQUIVALENT DEVICES

Function	Device with CMOS input	Device with TTL input
16×2-character alphanumeric LCD	Many variants	Devices such as LCM-S01602DTR/M
MOSFET driver	LM5100	LM5101
Vacuum-fluorescent-display driver	Many variants	Devices such as MM58342
CAN (controller-area-network) transceiver	PCA82C50	MCP2551
LIN (local-interconnect-network) transceiver	NCV7380	MCP201

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should consider increasing the pullup-resistor value. If the resistor value is too high, the diode bias current will be too low, and the diode may switch too slowly.

5V-TOLERANT INPUTS

Devices such as Microchip Technology's (www.microchip.com) new PIC24 family of 16-bit microcontrollers offer a unique feature to simplify the 5V interface. The devices offer 5V- or 5.5V-tolerant inputs, even when the device operates from a drain-to-drain voltage of 3.3V or less (**Figure 5**). These devices do not use clamp diodes that connect to the drain-to-drain voltage; they use a different mechanism to provide ESD protection. This feature is important for the 5V interface because it allows you to directly connect a 5V output to a 3.3V device without a resistor divider. If you revisit the example of **Figure 3**, you will see that this feature allows for a seamless 5V interface.

Some microcontrollers further enhance this feature by providing the option of generating a 5V output with an external 5V pullup resistor. The 3.3V device drives a 3.3V output, but it can tolerate a 5V input. The digitally controlled open-drain-output capability on these pins allows you to pull this pin to 5V without violating any specs. This feature supports a simple interface to 5V devices with CMOS inputs (**Figure 6**).

CAPACITANCE CAN LIMIT SPEED

When you use a pullup-resistor configuration, you must consider the maximum switching frequency and the capacitance of the connection between the two devices. Doing so helps determine the rise and fall rate of the signal on this port pin and the resistor value that is appropriate for the application. Consider the following equation:

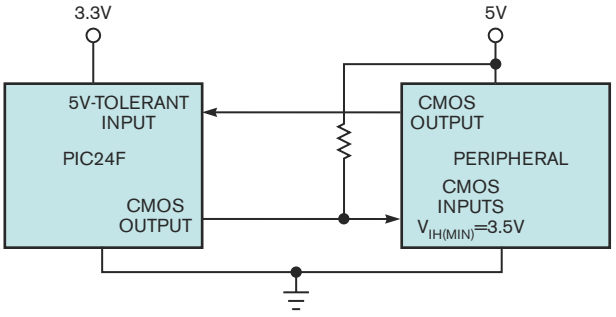


Figure 6 A pullup resistor on an open-drain output generates a 5V signal.

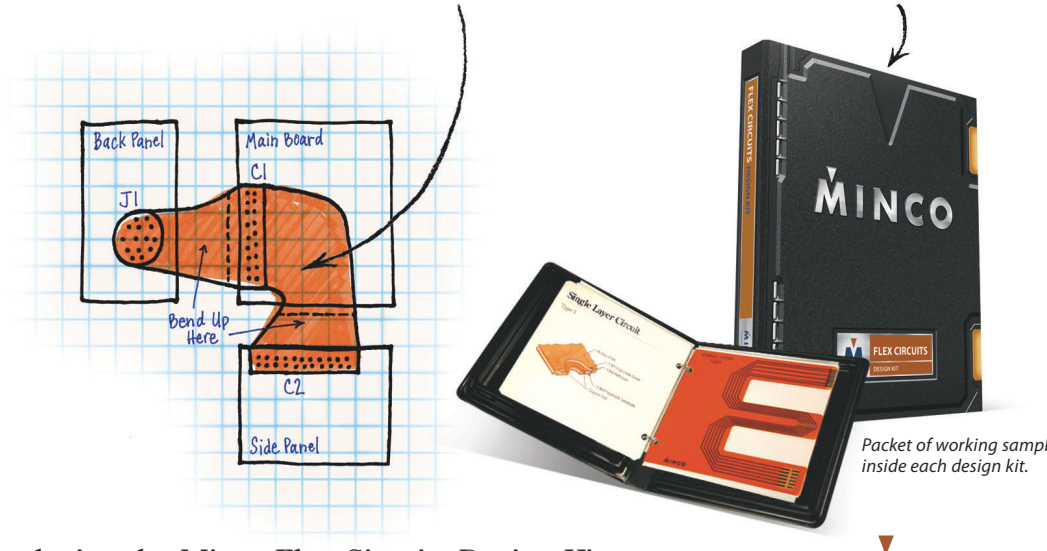
$$\text{RISE/FALL TIME} = \tau \ln\left(\frac{PV_{DD}}{PV_{DD} - PV_{IH(MIN)}}\right),$$

where τ is the RC time constant, R×C, PV_{DD} is the supply voltage of the peripheral, and $PV_{IH(MIN)}$ is the peripheral's minimum input high voltage. If you use a 1-kΩ pullup resistor, a 10-pF parasitic capacitance for the pin and pc board, the 5V supply

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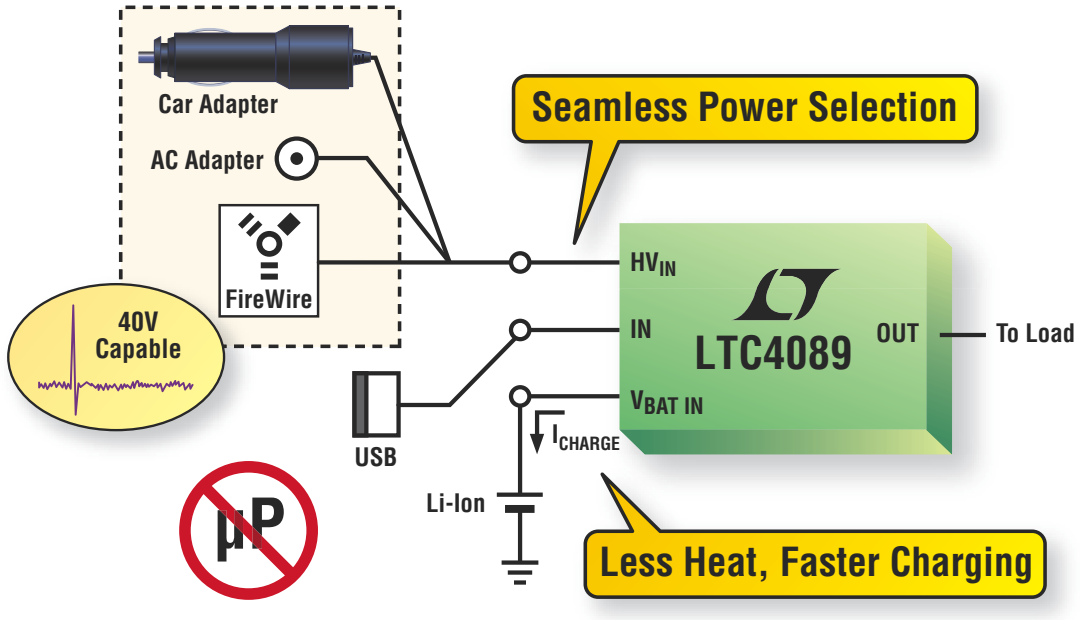
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LTC4055	1.25A	4.3V to 5.5V	Timer	4mm x 4mm QFN-16	PowerPath Control with Low Loss Ideal Diode
LTC4075	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter
LTC4076	950mA or 650mA USB	4.3V to 8V	C/x	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/5 USB Charge Current
LTC4077	950mA or 650mA USB	4.3V to 8V	C/10	3mm x 3mm DFN-10	Dual Input: USB or Adapter; C or C/x USB Charge Current

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voltage of the peripheral, and a 3.5V minimum input high voltage for the peripheral, the resulting rise and fall time will be approximately 12 nsec. If the minimum acceptable pulse width for this rise and fall time is 50 nsec, the maximum output frequency is 20 MHz, which is fast enough for most peripheral interactions.

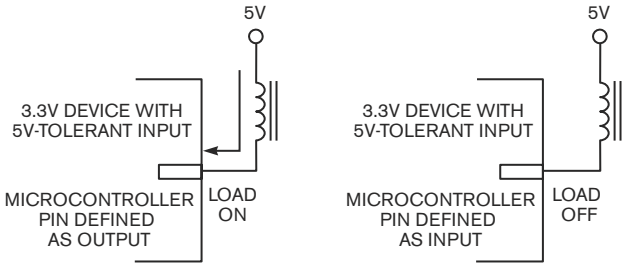


Figure 7 This circuit configuration drives low-impedance loads.

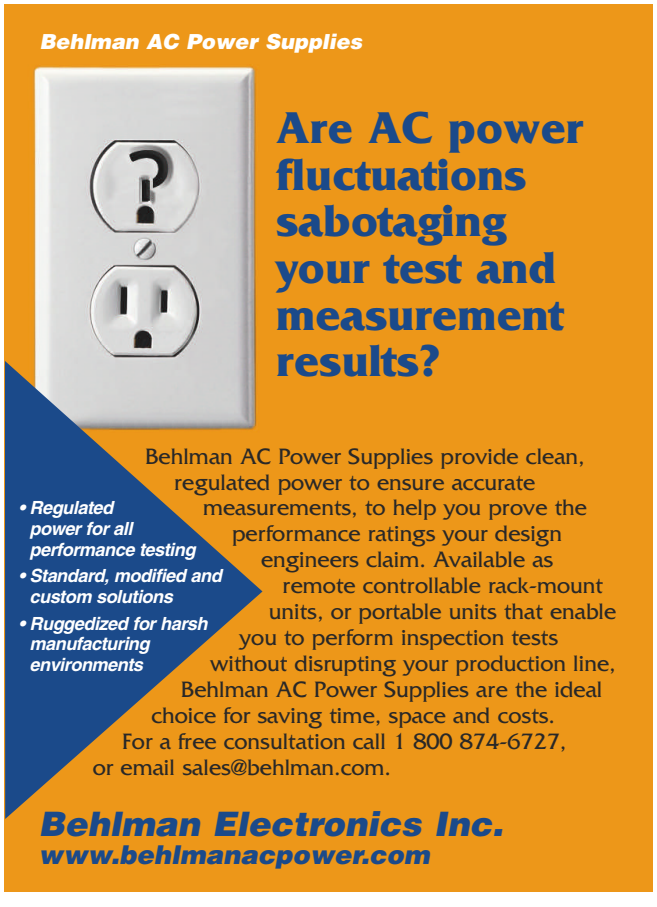
This configuration has a side effect: When the microcontroller drives the logic low, the extra current flows through a pullup resistor. The pullup resistor trades off speed for power-supply current. You need to select a compromise value for your application that provides the required speed and current consumption for the application.

Some may say that you can't use this kind of configuration to drive a low-impedance load. If you want to drive a 5V relay, what should you do? Fortunately, the previously described configuration is also helpful for driving low-impedance loads, such as relays. **Figure 7** shows the circuit-configuration information. To drive the load, define the pin as an output and drive it low. The only limiting factor is the device's current-sinking capability. To turn off the load, define the pin as an input, which turns off the load and applies 5V to the input. The pin tolerates 5V, so this operation is valid. In other words, you need to maintain a logic low on the output latch and toggle the input/output control register to turn the load on and off.

You now have an effective way to bridge 5 and 3.3V power-supply rails. You can devise similar low-cost, intelligent approaches for bridging other supply-voltage combinations during the transition to new, lower voltages. It is likely that most devices will soon move to lower voltages, eliminating the need for bridging. In the meantime, however, these methods should help you to lower your system costs by taking advantage of the newest semiconductor-industry trends. EDN

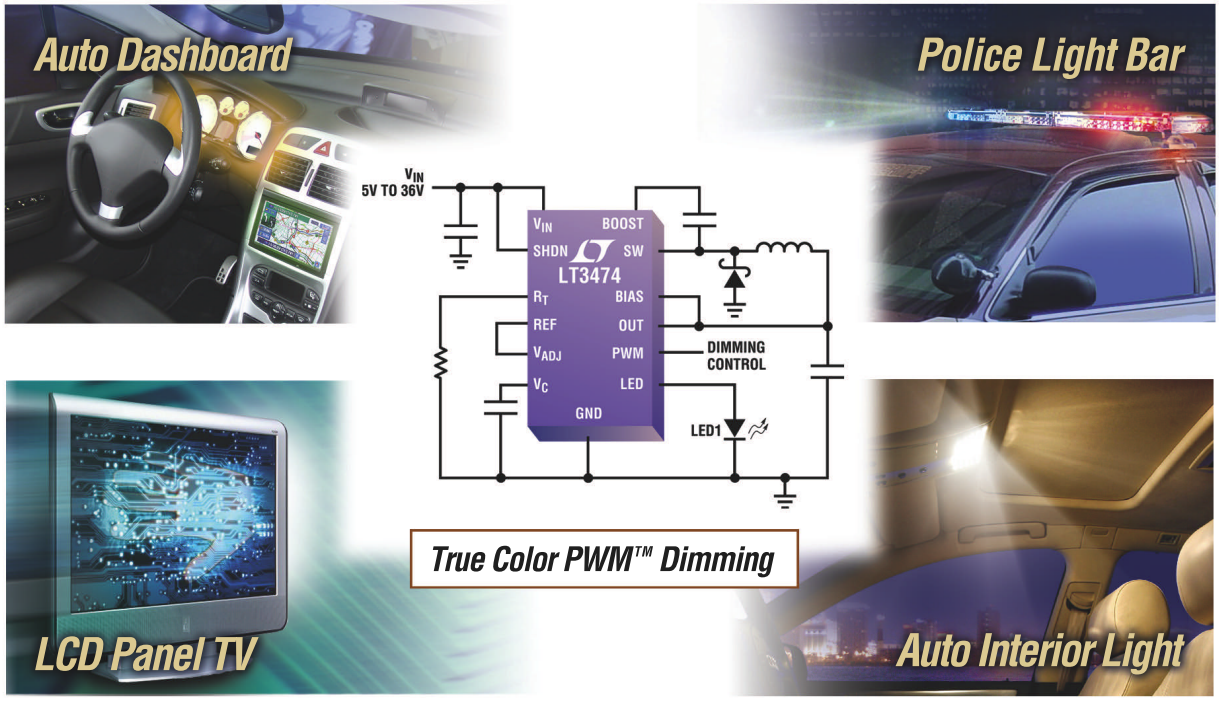
AUTHOR'S BIOGRAPHY

Gaurang Kavaiya leads the microcontroller-systems applications group supporting most PIC24, PIC18, and PIC16 products at Microchip Technology (Chandler, AZ). He has 10 years of experience in various areas of embedded-system design and has done assembly- and C-language programming and embedded-hardware design. He has also worked on Microchip's nanoWatt Technology power-management products, both as a manager and an engineer.





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LT3479	Boost	2.5V to 24V	1.5A	TSSOP-16E, DFN-14
LT3486	Boost	2.5V to 24V	0.35A x 2	TSSOP-16E, DFN-16
LTC3783	Boost/Buck/ Buck-Boost	3V to 36V	>1.5A Controller	TSSOP-16E, DFN-16

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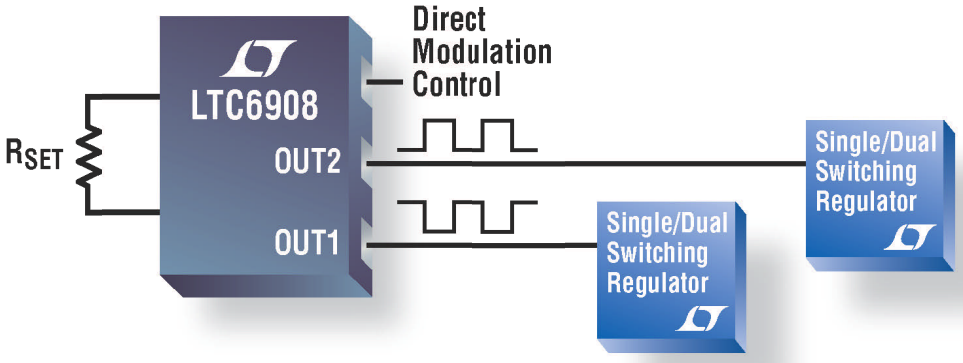
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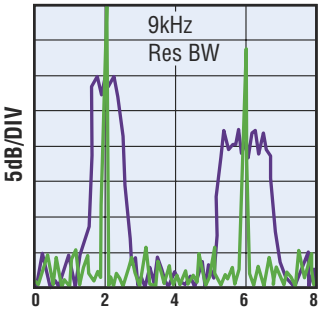
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DESIGN NOTES

Tracking and Sequencing Made Simple with Tiny Point-of-Load Circuit – Design Note 389

Scott Jackson

Introduction

Multiple-voltage electronics systems often require complex supply voltage tracking or sequencing, which if not met, can result in system faults or even permanent failures in the field. The design difficulties in meeting these requirements are often compounded in distributed-power architectures where point-of-load (POL) DC/DC converters or linear regulators are scattered across PC board space, sometimes on different board planes. The problem is that power supply circuitry is often the last circuitry to be designed into the board, and it must be shoehorned into whatever little board real estate is left. Often, a simple, drop-in, flexible solution is needed to meet these requirements.

The LTC®2927 provides a simple and versatile solution in a tiny footprint for both tracking and sequencing without the drawbacks of series MOSFETs. Furthermore, power supply stability and transient response remain unaffected because the LTC2927 offsets the output voltage of the regulator without altering the power supply control loop dynamics.

Basic Operation

Each POL converter that must be tracked or sequenced can have a single LTC2927 placed at point-of-load as shown in Figure 1. By selecting a few resistors and a capacitor, a supply is configured to ramp up and ramp down with a variety of voltage profiles. The choice of resistors can cause a slave supply to track the master signal exactly or with a different ramp rate, voltage offset, time delay, or combination of these.

Figure 2 shows a 4-supply tracking and sequencing profile that highlights the flexibility of the LTC2927. A master signal is generated by tying a capacitor from the RAMP pin to ground or by supplying another ramping signal to be tracked. This ramping signal can be a master signal generated by another LTC2927 or another tracking controller such as the LTC2923. Likewise, another supply voltage can be used as the master signal. If an external ramping signal is used, it can be connected directly to the RAMP pin or to the resistive divider connected to the TRACK pin.

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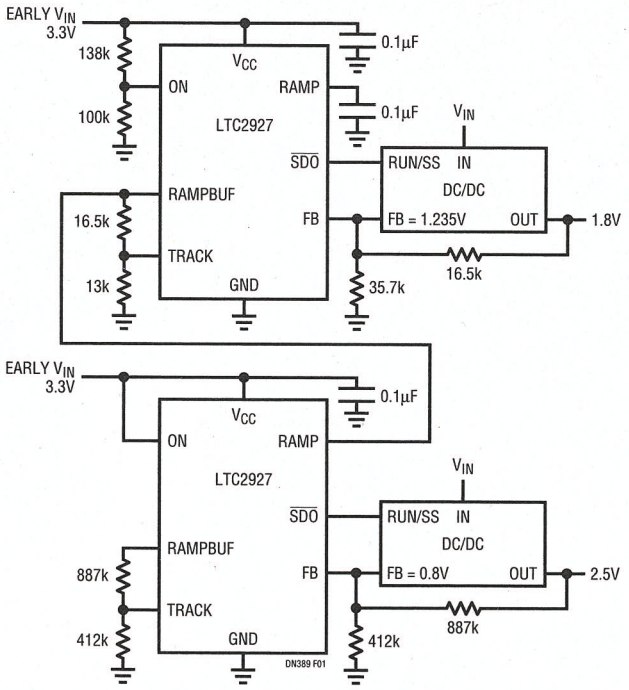


Figure 1. Dual Supply Tracking Application

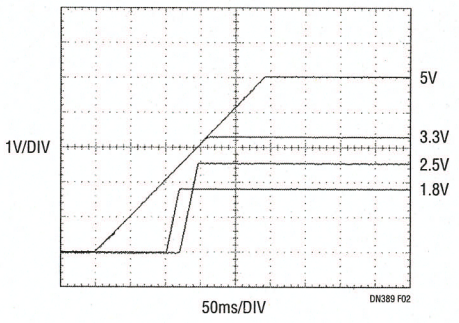


Figure 2. Output Profile of a 4-Supply System Showing Tracking, Sequencing and Ramp Rate Control

For applications that require master control of the shutdown or RUN/SS pins of the slave supplies, the LTC2927 provides an SDO output. SDO pulls low when the ON pin is below 1.23V and the RAMP pin is below 200mV.

Negative Supply Tracking

The LTC2927 can also be used to track negative voltage regulators. Figure 3 shows a tracking example using an LT3462 inverting DC/DC converter to produce a –5V supply. This converter has a ground-based reference, which allows current to be pulled from a node where R_{FA} has been divided. To properly pull current from the LT3462 FB network, a current mirror must be placed between the LTC2927 and the converter. Figure 4 shows the tracking profile of Figure 3 with a ramp rate of 100V/s. V_{MASTER} is positive, but the inverse is shown for clarity. The –5V slave does not pull all the way up to 0V at V_{MASTER} = 0V because the ground referenced current mirror cannot pull its output all the way to ground. If the converter has an FB reference voltage greater than 0V or if a negative supply is available for the current mirror, the offset can be removed. Figure 5 shows the resulting waveform.

Conclusion

The LTC2927 simplifies power supply tracking and sequencing by offering superior performance in a tiny point-of-load footprint. Only a few resistors are needed to configure simple or complex supply behaviors. Series MOSFETs are eliminated along with their parasitic voltage drops and power consumption. The LTC2927 offers all of these features in tiny 8-lead ThinSOT™ and 8-lead (3mm × 2mm) DFN package.

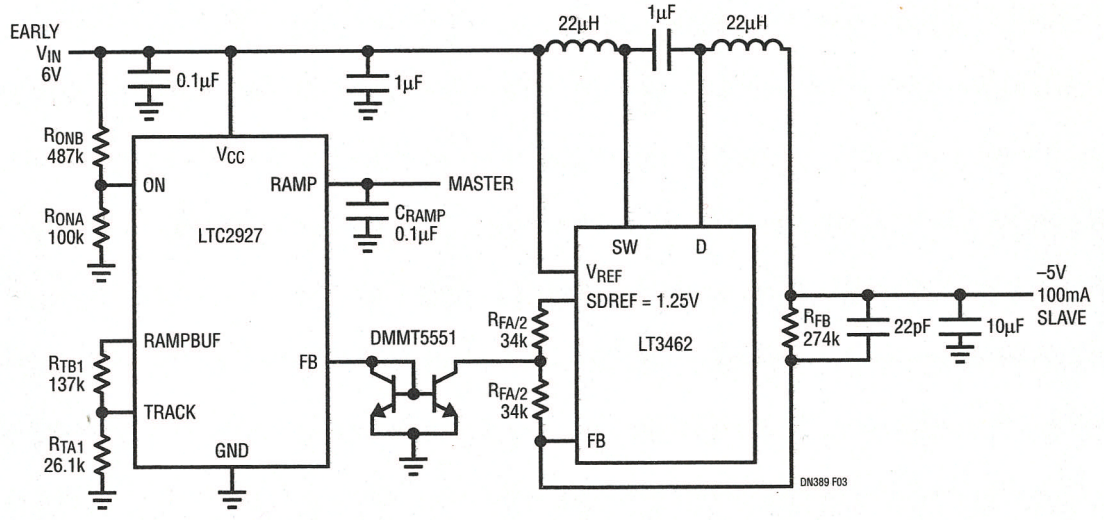


Figure 3. Supply Tracking of a GND Referenced Negative Regulator

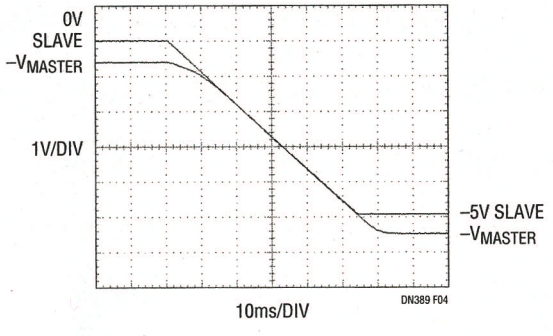


Figure 4. Tracking Profile of the Negative Regulator Application in Figure 3

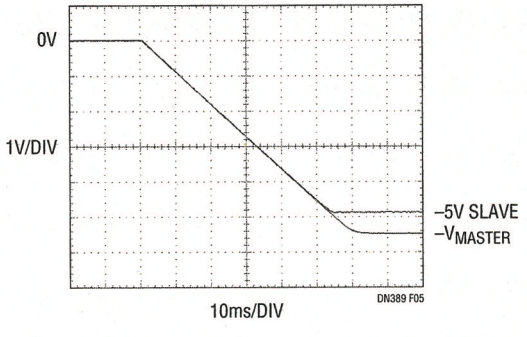


Figure 5. Tracking Profile of the Negative Regulator Application Without the Current Mirror Pull-Down Limitation

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READERS SOLVE DESIGN PROBLEMS

JFET-based dc/dc converter operates from 300-mV supply

Jim Williams, Linear Technology Corp, Milpitas, CA

You use a JFET's self-biasing characteristics to build a dc/dc converter that operates from power sources such as solar cells, thermopiles, and single-stage fuel cells, all of which deliver less than 600 mV and sometimes as little as 300 mV. **Figure 1** shows the drain-to-source characteristics of an N-channel JFET under zero-bias conditions, which you can produce by connecting its gate and source together. Applying 100 mV causes a current of 10 mA to flow through the device, increasing to 30 mA at 350 mV. Exploiting the JFET's ability to conduct significant current at zero bias makes it possible to design a self-starting, low-input-voltage converter.

The circuit can supply 5V at currents as large as 2 mA—enough to serve many micropowered applications or to provide auxiliary bias for a higher power switched-mode voltage regulator. At 300-mV input, the circuit starts up at load currents of 300 μA. A load current of 2 mA requires an input of 475 mV.

In **Figure 2**, Q_1, a parallel-connected pair of Philips Semiconductor's (www.semiconductors.philips.com) BF862 JFETs, and Coiltronics' (www.coiltronics.com) Versa-Pac transformer, T_1, form an oscillator in which T_1's secondary winding provides feedback to Q_1's gate. When you first apply power, Q_1's gate rests at 0V, and drain current flows through T_1's primary winding. T_1's phase-inverted secondary winding responds by delivering a negative voltage to Q_1's gate, which turns off Q_1 and interrupts current flow through T_1's primary winding. In turn, T_1's secondary voltage collapses, and sustained oscillations begin. Although the BF862's published specifications do not cover the device's internal geometry, the device has a low on-resistance and maintains a low gate-turn-on threshold voltage. Using a pair of parallel-connected JFETs for Q_1 ensures the low saturation voltage for operation at low power-supply voltages.

Rectifying and filtering the positive-going flyback-voltage impulses on Q_1's drain produce a dc voltage across capacitor C_1. To assist the circuit's start-up, a P-channel MOSFET, Q_2, which requires a gate-to-source voltage of approximately 2V for conduction, initially isolates the output load from the rectifier. When Q_2 conducts, the output voltage increases toward 5V. Comparator IC_1, a Linear Technology (www.linear.com) LTC-1440, draws power from Q_2's source and imposes output-voltage regulation by comparing its internal voltage reference with a sample of the output voltage. The output

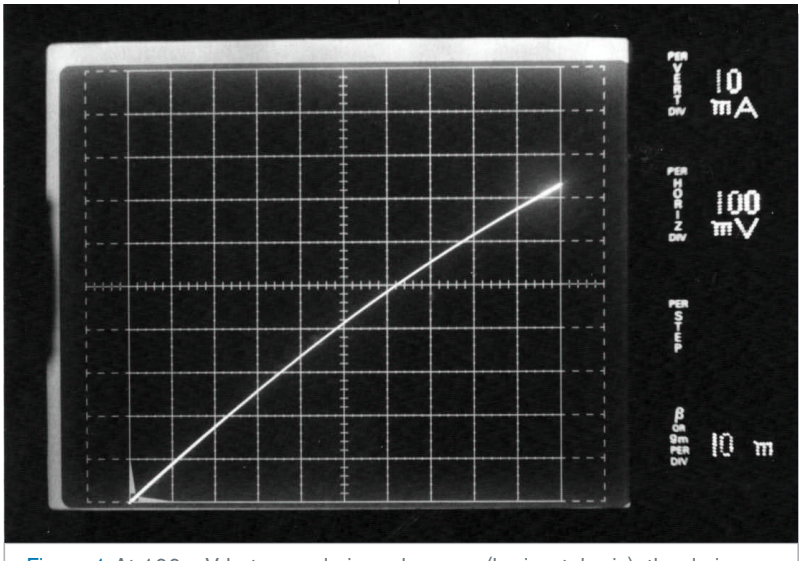


Figure 1 At 100 mV between drain and source (horizontal axis), the drain current reaches 10 mA (vertical axis) and increases to 30 mA at 300 mV.

DIs Inside

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from IC_1 varies Q_1's on-time through Q_3 to close the control loop and maintain output-voltage regulation. **Figure 3** shows the ripple voltage present at the power supply's output. When the output voltage decays, comparator IC_1 switches (Trace B, middle) and allows Q_1 to oscillate. The resulting flyback events at Q_1's drain (Trace C, bottom) restore the output voltage.

Using Q_3 as a simple but effective shunt control for Q_1's gate voltage results in a 25-mA quiescent-current drain from the power source. A modification reduces the quiescent drain to 1 mA (**Figure 4**). Inserting switch Q_4 in series with T_1's secondary winding more efficiently controls Q_1's gate. Bootstrapping the voltage across T_1's secondary winding produces negative-turn-off-bias voltage for Q_4. **Figure 5** illustrates how to connect T_1's wind-

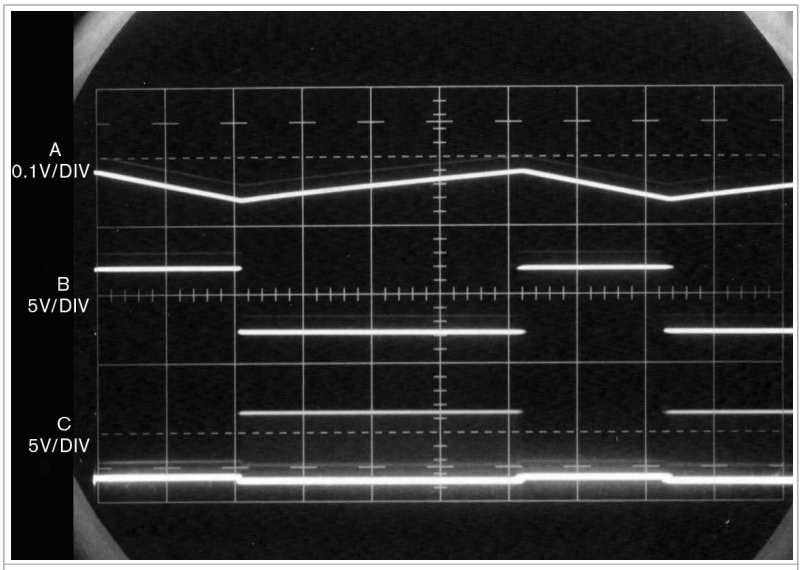
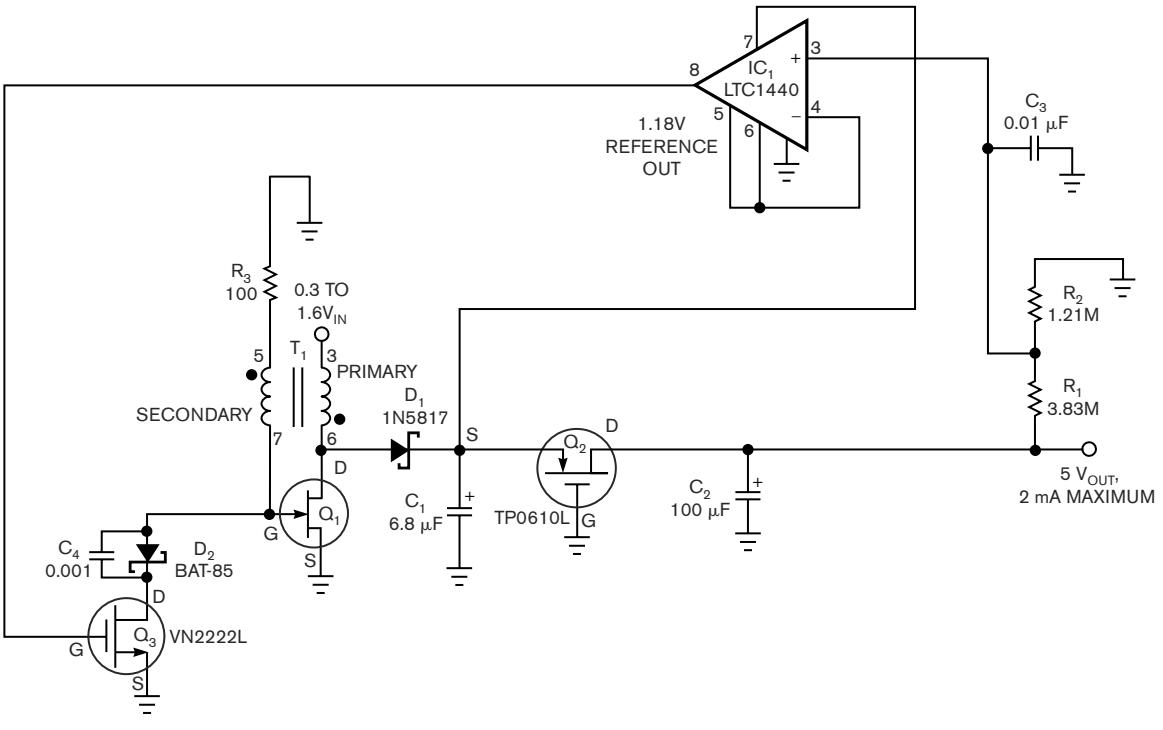


Figure 3 The dc output (Trace A), comparator IC_1's output, and the voltage at Q_1's drain (Trace C) have a horizontal-deflection factor of 5 msec.

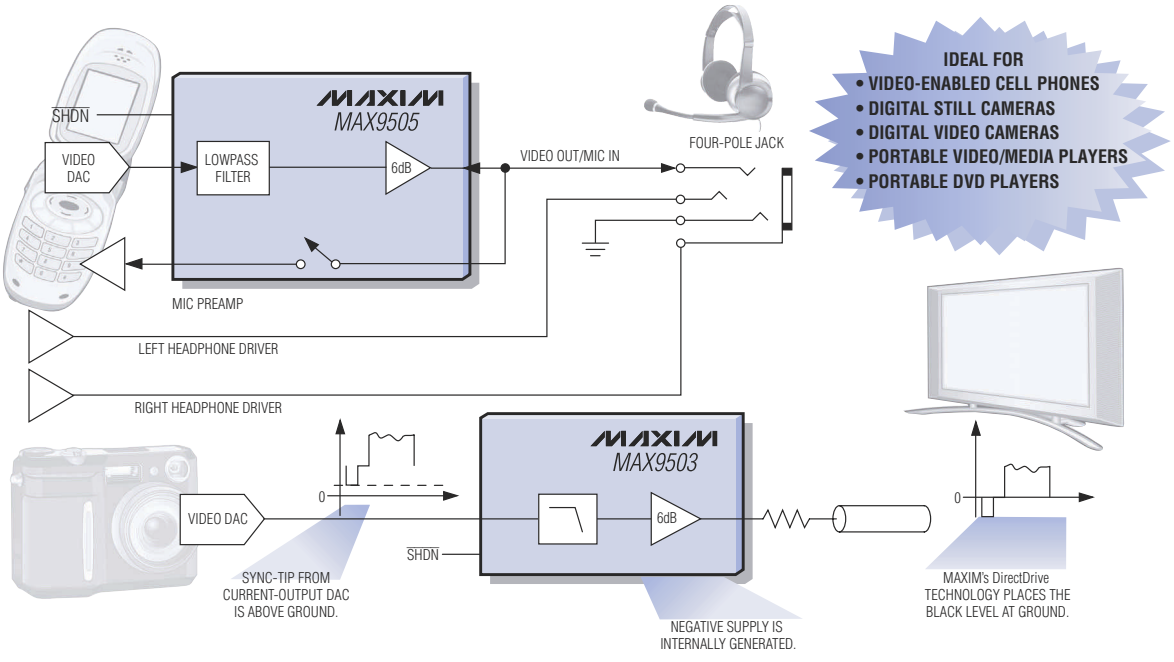


NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.

Figure 2 A pair of parallel-connected JFETs allows this dc/dc converter to operate from power sources that supply as little as 300 mV.

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MAX9505	DC	DC	Yes	6	2.7 to 3.6	10	16-QSOP/16-TQFN (3mm x 3mm)

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ings. When Q_4 switches off, it interrupts the current flowing in T_1's secondary winding and drives T_1's Pin 5 positive. Without diodes D_4 and D_5, the peak voltage would approach 15V and reverse-bias Q_4, an undesirable condition. Under normal operating conditions, excursions of approximately 0.8V appear at Pin 5, necessitating the use of two series-connected diodes to clamp the voltage at a safe level. Zener diode D_3 holds off bias-supply loading to aid start-up during initial power application.EDN

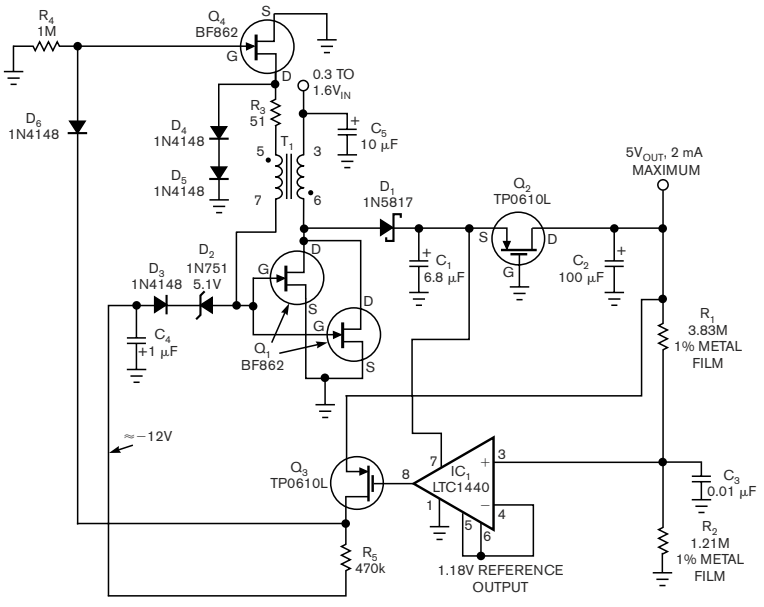


Figure 4 Adding Q_3, Q_4, and the bootstrapped negative-bias generator comprising D_2, D_3, and C_4 reduces the circuit's quiescent current from 25 mA to 1 mA.

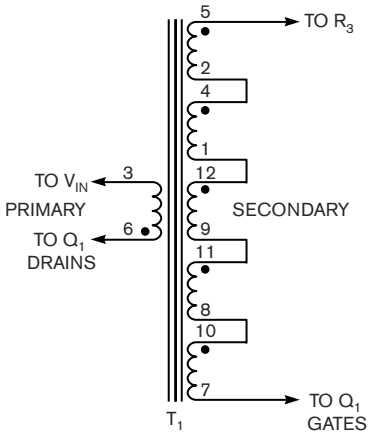


Figure 5 Comprising six independent windings that offer more than 500 configurations, Coiltronics' VP1-1400 serves as a combination feedback and flyback transformer in this application. Connect the windings as shown.

Configurable logic gates' Schmitt inputs make versatile monostables

Glenn Chenier, Allen, TX

You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (**Reference 1**) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

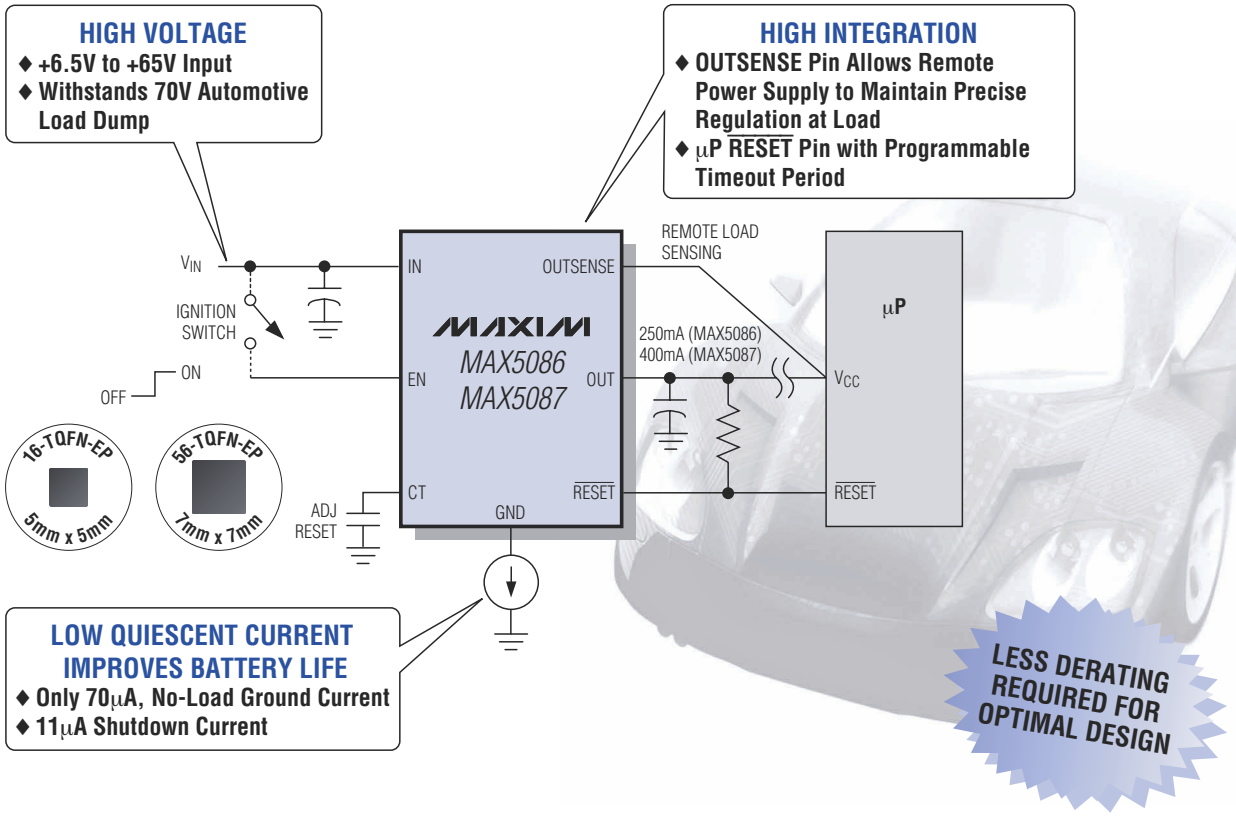
Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (**Reference 2**) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

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offers functional equivalents—the SN74LVC1G57 and SN74LVC1G58 (**Reference 3**). Both companies' devices offer upper- and lower-trip-point-voltage thresholds averaging 37 and 63%, respectively, of V_{CC}, or approximately one RC time constant on the rising or the falling edges. According to the published data sheets from the manufacturers' Web sites, Texas Instruments' versions impose somewhat tighter tolerances on the analog threshold levels and thus deliver tighter timing tolerances than do the Fairchild parts.

For digital-analysis purposes, any voltage below the upper trip point for a rising edge effectively represents a logic zero, and any voltage above the lower trip point for a falling edge represents a logic one. These conditions are true only after the input crosses a respective trip point, such as a rising edge that approaches but never crosses the upper trip point. This voltage remains a logic zero, even if the voltage then drops back to ground potential on its falling edge.

Figure 1a shows some typical circuit implementations. Note that these circuits lack some of the niceties of genuine monostables. For example, a circuit doesn't retrigger until after its RC network has stabilized or about five time constants have elapsed. The RC time constant must be five times shorter than the time between triggering events. Devices from the SN74LVC1G57 family produce the waveforms in **Figure 1b**, and circuits using the SN74LVC1G58-family devices produce the inverse of these waveforms. The circuits' operation is straightforward. The RC circuits delay one input, so that the inputs momentarily rest at opposite states. When one RC time constant elapses, the delayed voltage crosses the Schmitt upper- or lower-trip-point thresholds, and the delayed input catches up to the straight-through input.

Of unusual interest and unlike the usual variety of monostable that triggers only from a voltage transition in one direction, the XOR implementation functions as a monostable triggered by both the rising and the falling edges, enabling it to function as a frequency doubler for generating strobe pulses on rising and falling clock edges. You can make any inverting-gate configuration into an oscillator by feeding back its inverted output to an RC-delayed Schmitt input and enabling the gate's remaining input. However, once the XOR oscillator's remaining gate switches off the oscillation, the gate's output state hangs at either a one or a zero to produce a truly random state derived from the oscillation's nonsynchronous relationship to the timing of the disabling input. EDN

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2. "NC7SZ57/NC7SZ58, TinyLogic UHS Universal Configurable 2-Input Logic Gates," Fairchild Semiconductor, April 2000, www.fairchildsemiconductor.com/ds/NC/NC7SZ57.pdf.
3. "SN74LVC1G57 Configurable Multiple-Function Gate," Texas Instruments, November 2002, http://focus.ti.com/lit/ds/symlink/sn74lvc1g57.pdf.

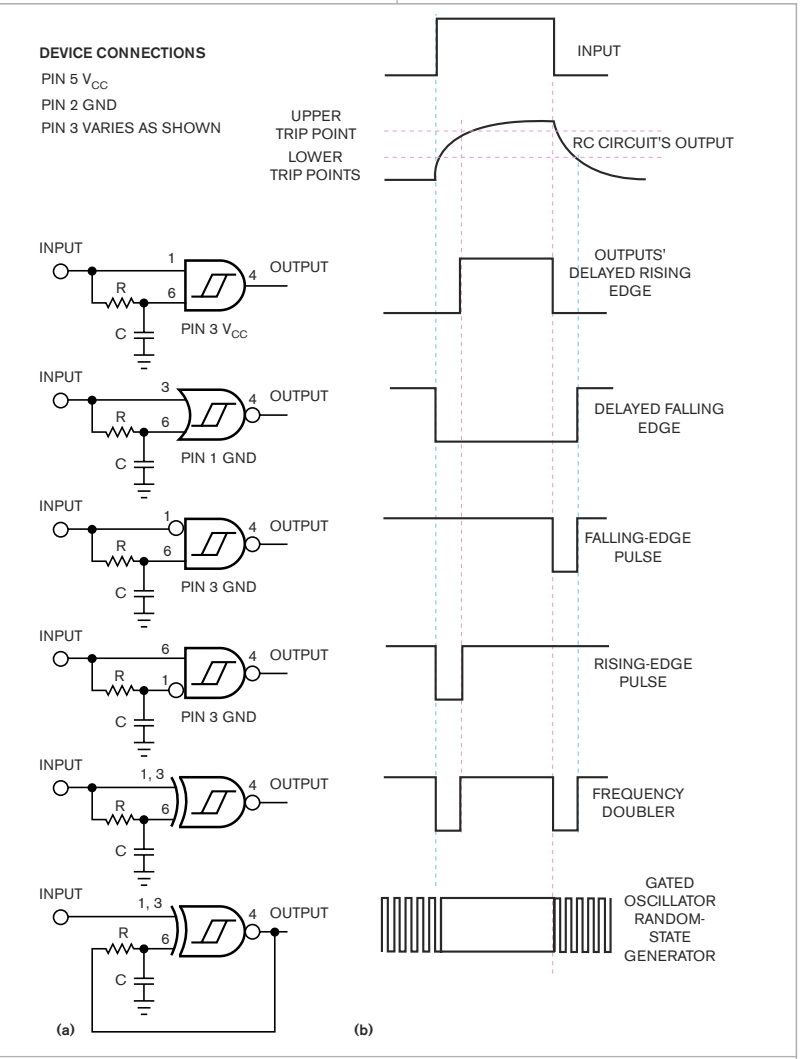
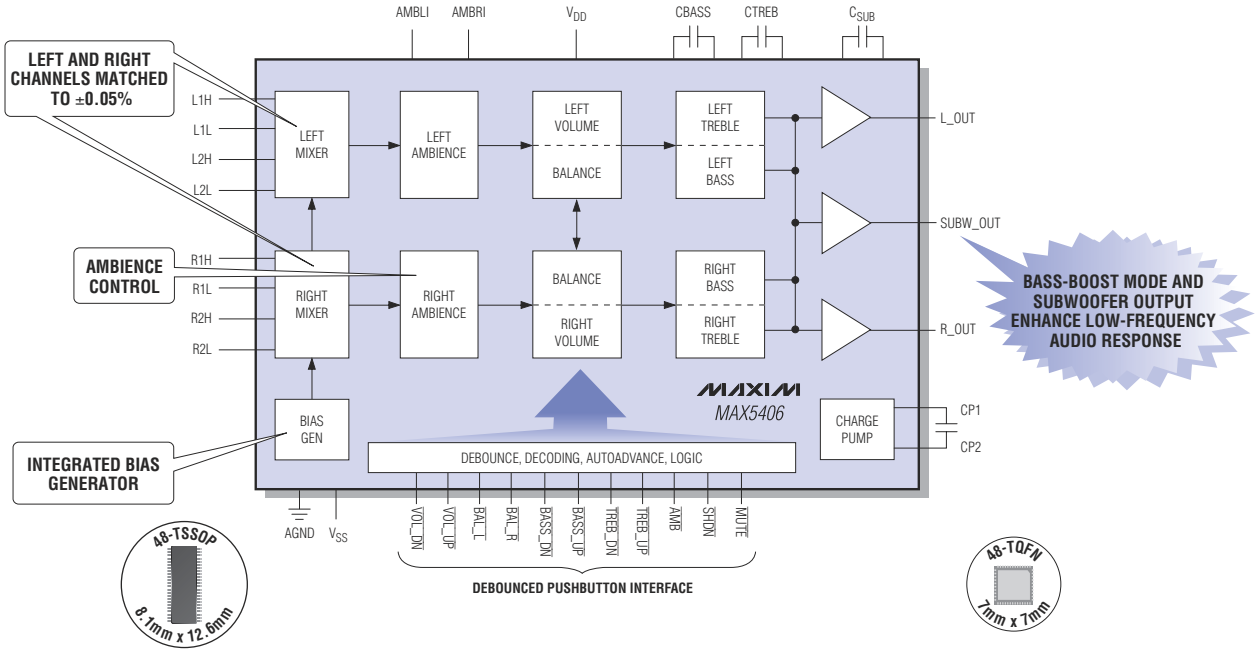


Figure 1 One gate plus an RC network (a) can deliver a range of useful timed outputs (b).

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Stealth-mode LED controls itself

Howard Myers, Greensboro, NC

Since the LED's invention more than 30 years ago, its emission efficiency has steadily increased, and, although it may surprise you, the increased conversion efficiency works in two directions. Certain bright, efficient LEDs, such as Hewlett-Packard's (www.hp.com) HLMP-EG30-NR000, a red emitter molded in clear encapsulation, also exhibit significant photovoltaic action. The circuit in **Figure 1** shows how you can put an LED's photovoltaic characteristics to work. Using the same components, older, red LEDs also function but with lower light output in this circuit. This Design Idea circuit describes an LED that controls itself by determining whether it's on or off without the assistance of any light sensor other than its own characteristics. When you darken the LED, it turns on, and, when you illuminate it, it turns off. The circuit's main components comprise LED D_1, micropower operational amplifier IC_1, one-shot IC_{2A}, and transistor switch Q_1 to control current through the LED.

When dark, the LED produces no photovoltaic current. When moderate lighting, such as that in an office or a lab, illuminates it, it generates 50 to 100 mV into a 4.7-MΩ load resistor. Comparator op amp IC_1 compares the voltage that the LED produces with a threshold reference voltage of approximately 50 mV. You can vary the circuit's sensitivity threshold by altering the values of resistors R_1 and R_2 in the voltage divider that connects to IC_1's Pin 2.

When ambient light decreases, the LED produces less voltage, and, when the voltage falls below the 50-mV threshold, the op amp's output goes low and triggers one-shot IC_{2A}. The one-shot turns on transistor Q_1 for an interval, lighting the LED for approximately 3 msec until the one-shot's output goes low. In a darkened room, the cycle repeats at a 200-Hz rate, and the LED blinks repeatedly with short off periods. At high flash rates, the LED appears to be continuously on.

The circuit's current drain in the daylight state mainly comprises the current driving the reference-bias network: 3.6V/162 kΩ=22 μA. In both day and night modes, with the LED drawing a few milliamperes when illuminated, a battery that can deliver 1 Ahr would power the circuit for a couple of months. You can reduce the current by increasing the values of R_1 and R_2. Given the circuit's low and intermittent current drain in a well-lighted environment, a 1-Ahr lithium cell's service life should approach its shelf life. EDN

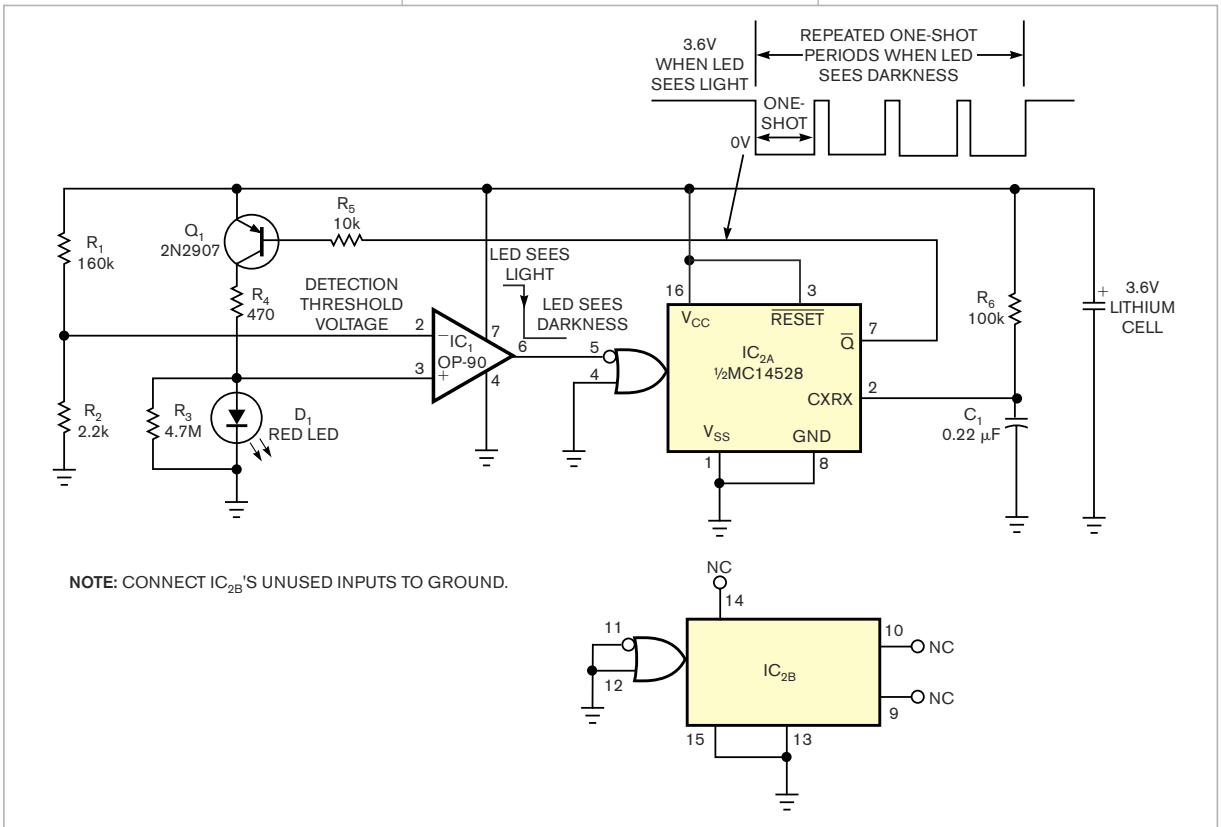


Figure 1 An efficient LED forms the heart of a light-sensitive "mystery lamp" that contains no apparent photodetector.

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	Vdc2	3.3 or 5	3.3 or 5
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	Iout-2 (A)	6/4	6/4
Input Voltage Range (VAC)		90-264	90-264
Isolation Voltage	Pri-Sec	3000Vrms	3000Vrms
	Pri-Chassis	1500Vrms	1500Vrms
PFC		Yes	Yes
Current Share		Active	Active
Efficiency		92%	92%
Features	HotPlug	Yes	Yes
	I^2C	Yes	Yes
	EMI Class	Class A	Class A
	Airflow Direction	Back or Front	Back-Front
	Input Connector	IEC 320 C15	IEC 320 C20
	Output Connector	FCI PowerBlade #51732-021	FCI PowerBlade #51732-021
Dimensions (WxLxH)	Inches	4.75 x 12 x 1.6	4.75 x 12 x 1.6
	mm	120,6 x 305 x 40,7	120,6 x 305 x 40,7
Datasheet Name		D1U-W-1200-12	D1U-W-1600-12

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Data-acquisition system captures 16-bit voltage measurements using the USB

Terry Millward, Maxim Integrated Products Inc, Blonay, Switzerland

The USB has become the interface of choice for connecting to PCs. Available on all relatively modern PCs, the USB offers a standard connector and can supply power to peripherals at 5V and as much as 100 mA of current. The circuit in **Figure 1** combines Maxim's (www.maxim-ic.com) MAX1168, a low-power, 16-bit ADC, with a small USB-interface module to make a simple, eight-channel, 16-bit measurement system. The MAX1168 includes eight input channels, an SPI (serial-peripheral-interface) port, a 4.096V reference, and a clock oscillator. The MAX1168 operates from a 5V supply and can convert individual channels, execute multiple conversions on one channel, or scan the channels sequentially and store measured data on-chip.

Based on a Cypress (www.cypress.com) CY7C63743 controller, USBmicro's (www.usbmicro.com) U421 USB-interface module provides as many as 16 I/O lines and an option to use some of those lines as an SPI port at selectable clock rates of 62.5 kHz, 500 kHz, 1 MHz, or 2 MHz. Firmware on the U421 allows generic access to SPI read-and-write devices, and the device's general-purpose I/O lines can serve as slave-select lines for addressing multiple SPI devices. One I/O line controls the MAX1168's chip-select input. When you use it with an

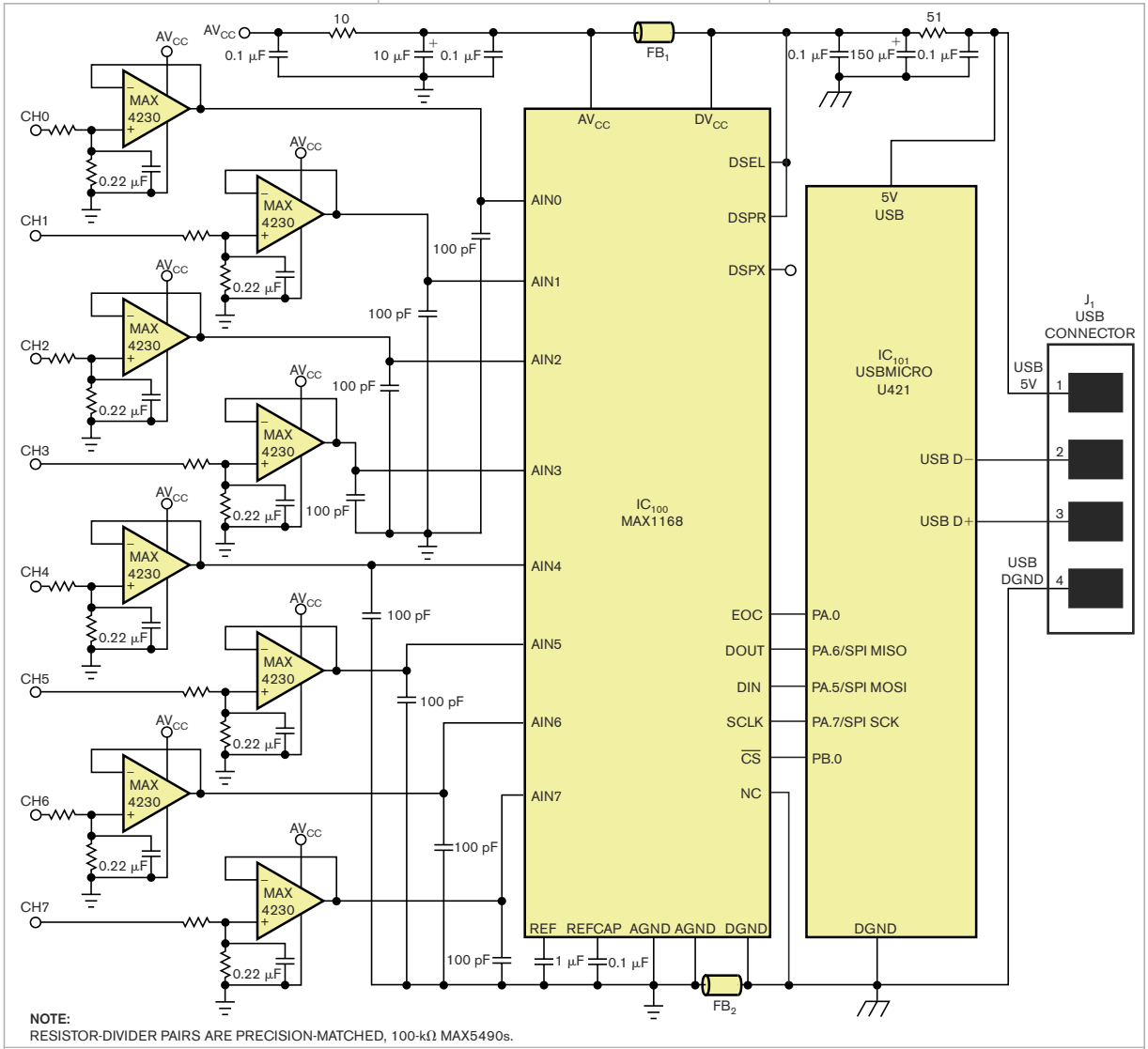


Figure 1 This simple data-acquisition system provides eight channels of 16-bit data to a host computer through a USB interface.

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Part Number	Type	Stability (ppm)	Frequency Range	Output Formats	Package Size	Supply Voltage
Si530	XO	±20 ±50	10 MHz–1.4 GHz	LVPECL LVDS CML CMOS	5x7mm	3.3 V 2.5 V 1.8 V
Si530	Dual XO					
Si534	Quad XO					
Si550	VCXO	±20 ±50 ±100	10 MHz–1.4 GHz	LVPECL LVDS CML CMOS	5x7mm	3.3 V 2.5 V 1.8 V
Si552	Dual VCXO					
Si554	Quad VCXO					

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HID (human-interface device), the U421 USB controller can transfer data at rates as high as 800 bytes/sec. With additional filtering to reduce noise, the USB port provides 5V power to the circuit.

The MAX1168's sample-and-hold circuit must acquire the input voltage and charge its 45-pF holding capacitor in 3 µsec and thus requires a fast amplifier to minimize acquisition errors. Available in dual and quad versions, the MAX4230 provides a 10-MHz bandwidth, 2V/µsec slew rate, rail-to-rail inputs and outputs, and the ability to operate from a 5V rail or from voltages as low as 2.7V. The MAX4230's bias current—typically, 50 pA—allows significant input impedance without affecting accuracy.

To provide protection from overvoltages and apply input-voltage scaling, each buffer amplifier's input includes a 100-kΩ precision-matched resistive divider. This application uses Maxim's MAX5490VA10000 10-to-1 dividers, which provide a scaling factor of 1/11, to allow maximum readable inputs of 45V at resolutions of 687.5 µV.

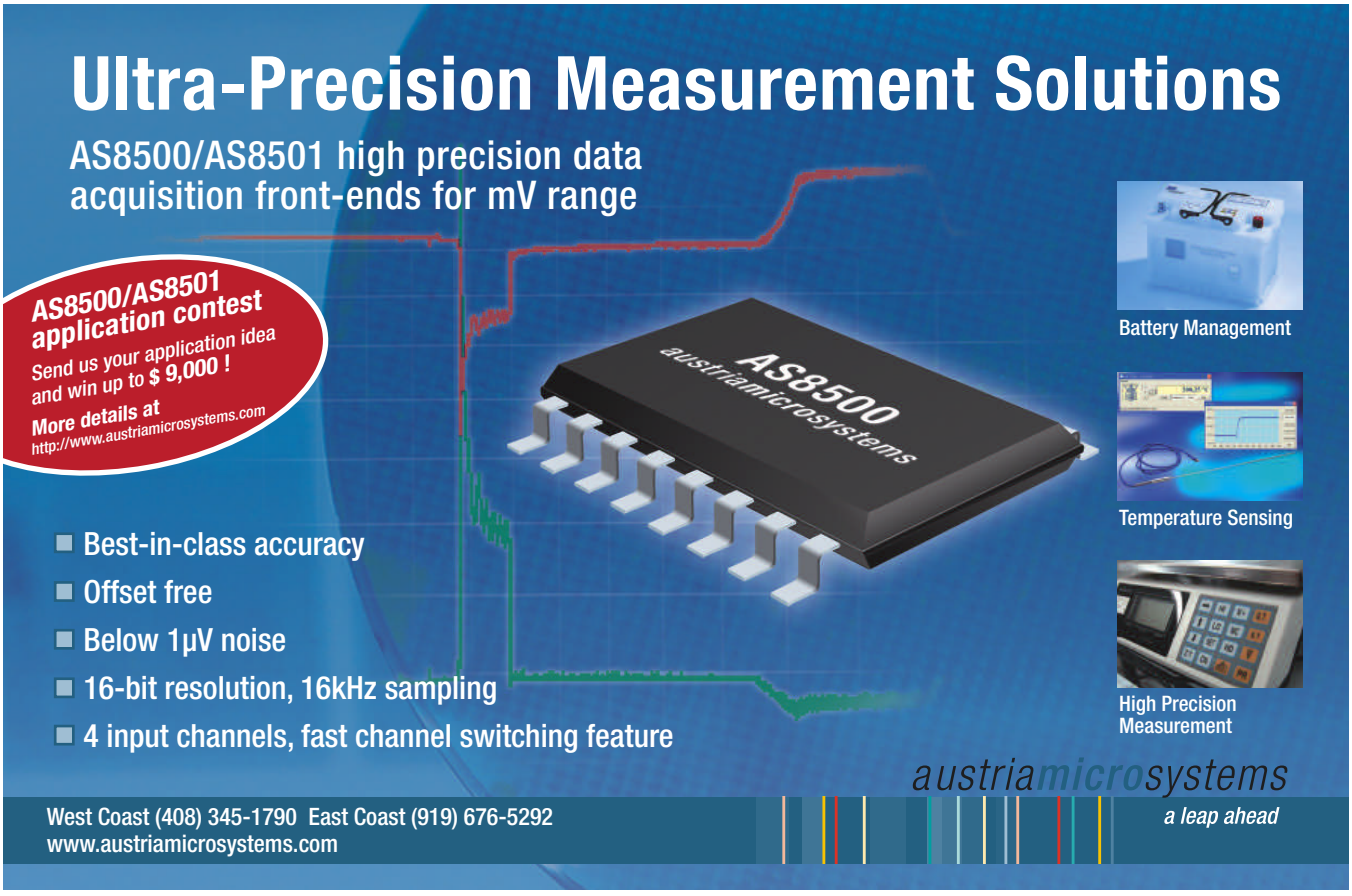


Figure 2 User-interface software for the data-acquisition system allows selection of operating parameters. In this image, the lower three channels are unselected and hence are not visible in the display.

Written in Microsoft's Visual Basic.Net, Standard Edition, the evaluation software provides commands to the U421 through the USBm.dll DLL (dynamic-linking-library) file. The demo program sets the MAX1168 to scan all eight channels and display the results. When you run the program, the Visual Basic form allows you to set the reference voltage to allow for the input divider, select the scan time, and enable any of the eight input channels for screen display (**Figure 2**). You can download the evaluation software at www.maxim-ic.com/MAX=1168DI.EDN

ACKNOWLEDGMENT

Thanks to Robert Severson of USBmicro for his help with the interface.



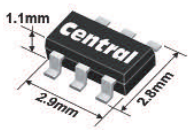
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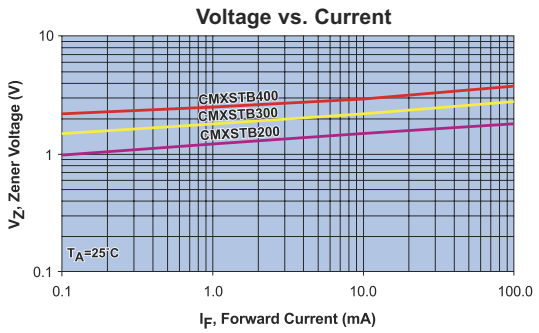
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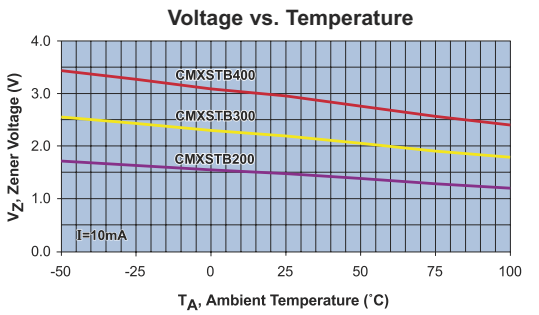
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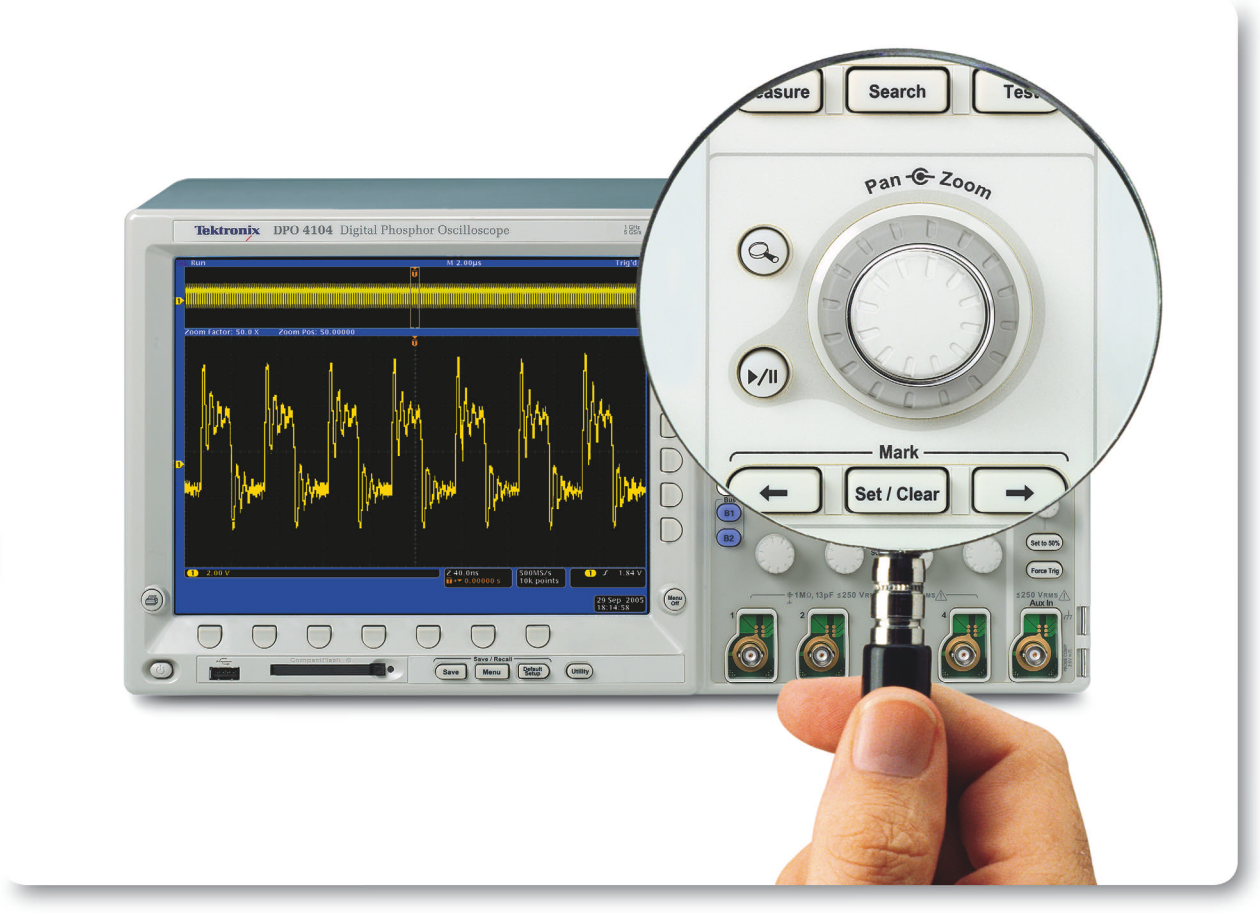


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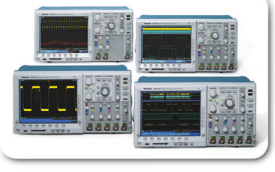
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Exceeding 90% efficiencies, the one-eighth-brick EMS series of dc/dc converters uses advanced-thermal-management techniques. These devices provide 70°C performance, requiring 200-lfm cooling for 5V-output-voltage full-power operation with 24 or 48V input voltage. Two single-output models deliver 3.3V at 15A and 5V at 10A from an 18 to 60V input range. The EMS series of one-eighth-brick converters costs $36 (1000).

Power-One, www.power-one.com

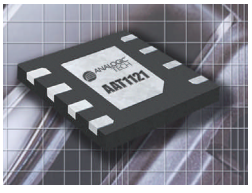
Low-voltage dc/dc converters provide high output current

Targeting high-end telecom, industrial, transportation, and military equipment, the single-output-isolated UWR 7-15W dc/dc-converter series comes in 1×2-in. packaging. Available in 1.2, 1.5, and 1.8V output voltages, the devices provide a 6A output current. Input voltages range from 9 to 18, 18 to 36, and 36 to 75V. Without the need for heat sinks or forced-air cooling, the converters have a −40 to +60°C temperature range. Combining a high-frequency, synchronous-rectifier topology with an SMT-on-pc-board construction provides an 88% efficiency. The UWR 7-15W series costs $35.

C&D Technologies, www.cd4power.com

Step-down converter targets Bluetooth headsets

Aiming at space-constrained portable devices, the AAT1121 step-down converter comes in 2×2× 0.85-mm TDFN packaging. Providing a 250-mA output current at 96% efficiency, the converter operates over a 2.7 to 5.5V input range with an output as low as 0.6V. Using a 1.5-MHz switching frequency, the device maintains a 30-µA no-load quiescent current. Targeting Bluetooth headsets and ultrathin digital still cameras, the AAT1121 step-down converter costs 76 cents (1000).



Advanced Analogic Technologies, www.analogictech.com

Small dc/dc converters feature true shutdown

Using an inrush current to save battery life, the dual-output, MAX-8614 step-up dc/dc converter also includes a pin-selectable CCD power-up sequence, eliminating external timing circuits. The converter generates +24V-positive- and −10V-negative-voltage outputs with a 100-mA output current and an

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POWER SOURCES

adjustable output using external resistors. Targeting digital still cameras, mobile-phone cameras, and OLED-display power, the device also features true shutdown without an external FET or internal compensation capacitors. Available in a 3×3-mm TDFN-14 package, the device costs $2 (1000).

Maxim Integrated Products, www.maxim-ic.com

PFC controller reduces power loss

This active PFC (power-factor-correction)-controller IC reduces power by 320 mW in SMPS (switch-mode-power-supply) designs consuming less than 250W, such as notebook adapters. Operating in CRM (critical-conduction mode), the FAN7528 integrates a dual-output-control function to increase efficiency with a universal ac input. The input renders unnecessary the sensing of the rectified ac-line voltage for PFC, providing a drop in standby power. Available in a lead-free package, the FAN7528 PFC controller costs $1 (1000).

Fairchild Semiconductor, www.fairchildsemi.com

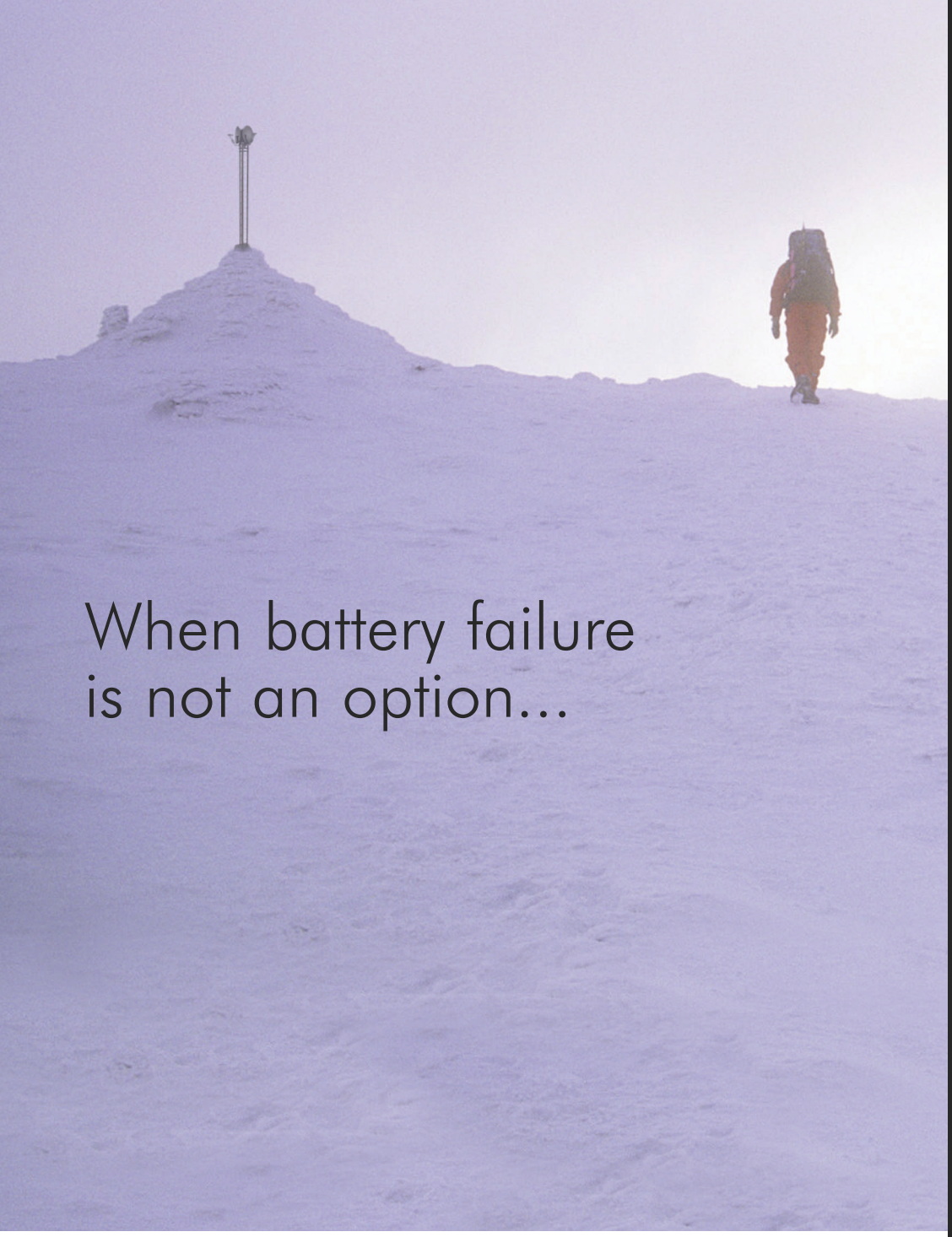
Buck-voltage regulator powers graphics-processing units

Using mobile-voltage positioning, the ISL6263 single-phase buck-voltage regulator powers next-generation graphics-processing units and Santa Rosa-platform graphics cores. The device reduces power consumption and enhances processor performance by changing output voltage and operation modes corresponding to the advanced graphics-control protocol. The vendor's ISL6263 5-bit VID (voltage-identification) regulator provides 0.5% system accuracy throughout the temperature range, allowing a wider tolerance of inductors for platforms using dc-resistance sensing. To boost battery life, the battery can use lower switching frequencies at discontinuous-conduction mode through internal automatic inductor-current sensing or VID programming. Available in a QFN-32 lead package, the ISL6263 costs $2.70 (1000).



Intersil Corp, www.intersil.com

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productroundup

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500W C-Bus converter runs without heat sink

Delivering 42A in a 12V-nominal output, the CBQ4248G1 C-Bus 500W intermediate-bus converter runs at 97% efficiency without a heat sink. This quarter-brick suits datacom, networking, and automatic-test-equipment applications using a two-stage power-conversion architecture at 48 ac and 48 to 12V dc. Additionally, the converter features an unregulated 12V-dc isolated intermediate-bus voltage. Available in both open-frame and baseplate versions, the CBQ-4248G1 C-Bus costs $48.

Cherokee International, www.cherokeepwr.com

TEST & MEASUREMENT

Small spectrum analyzer troubleshoots wireless networks

The 2.4-GHz Wi-Spy spectrum analyzer can visually display many wave types and stores real-time data for later reference. This ability suits the tool for troubleshooting wireless networks or optimizing WLAN-signal strength. Comparable in size with a small flash drive, the Wi-Spy USB-key device costs $99.

MetaGeek, www.metageek.net

Debugging device ports from Linux using USB 2.0

Using the usb2Demon and the vendor's debugging interface, users can port the OCDemon on-chip-debugging technology to a Linux platform. A user can debug, test, and program hardware and software in Linux and then port to the target system over a USB 2.0 connection. The usb2Demon costs $750, and several free downloadable tool sets are available for Linux and Windows.

Macraigor Systems, www.macraigor.com

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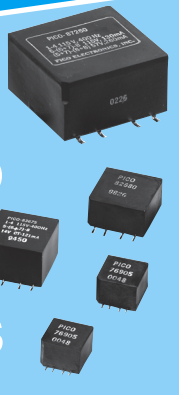
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Measurement platform comes in a variety of bundles

Measuring semiconductor wafers, ICs, pc boards, MEMS, and bioscience devices, the M150 measurement platform allows users to switch between devices in minutes. Interchangeable standard parts make this 150-mm measuring device customer-configurable, allowing the platform to address problems including power consumption, operating frequency, signal isolation, signal integrity, and channel bandwidth. The platform is compatible with the vendor's L-Series microfluidics-metrology systems and all L-Series life-science applications. Platforms are available in application-specific, preconfigured packages for dc, RF, failure analysis, pc-board test and millimeter wave, or in a user-customized format. Prices for the M150 measurement platform range from $7000 to $45,000.
Cascade Microtech, www.cascademicrotech.com

INTEGRATED CIRCUITS

Audio DSP features true parallel processing

Using a dual-core structure, the CS49530 audio DSP family operates as two high-performance DSPs in a single IC. Providing true parallel processing, the family has 1.8 Gbytes of processing power. The availability of on-chip RAM and ROM eliminates the need for external memory. The CS-495313-CQ4 costs $12.95 (10,000) in an LQFP-144; the CS495303-CQ8 and S495313-CQ8 cost $9.95 and $11.95 (10,000), respectively, and come in LQFP-128 packages.
Cirrus Logic Inc, www.cirrus.com

DSP family adds inexpensive versions

Adding to the vendor's Aureus line of high-performance audio DSPs, the TMS320DA707 and TMS-320DA705 processors are the lowest priced parts in the product family. Providing high-quality audio, these DSPs target low-end and midrange applications requiring multichannel decoding. Both devices are software-compatible with all DA7xx and previous-generation DA6xx devices and are pin-compatible with the DA708. The DA707 DSP supports off-chip SDRAM. These 250-MHz devices come in TQFP-144 packages. The TMS320-DA705 and TMS320DA707 DSPs cost $9.23 and $11.33 (10,000), respectively.
Texas Instruments, www.ti.com

SOCs support standard- and high-definition decoding

Targeting low-end and midrange digital-television markets, the TC90400XBG and TC90400FG SOCs (systems on chip) use a 64-bit, MIPS-based RISC host processor and three DSPs. Able to decode multiple standard-definition streams or single high-definition streams, the chips can display in 720×480-pixel, 960×1080-pixel, or 1080i resolution. The chips can output standard 480i analog output and support a unified 16-bit DDR-memory system as well as a NAND and NOR flash-memory controller. Additional features include a 180-MHz TX49/L3 core; a transport-stream processor; a built-in audio processor with MPEG-audio, Dolby AC-3, and AAC decoding; and a graphics engine with two planes. In addition, the TC90400XBG supports hard-disk-drive applications. Prices for the TC90400-XBG and TC90400FG range from $10

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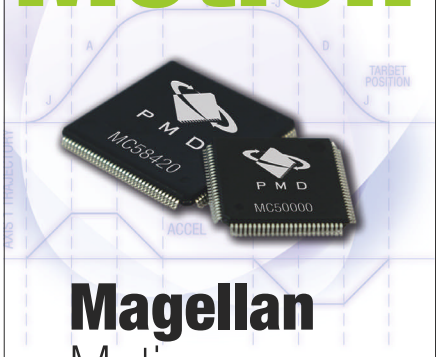
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to $18 (100,000), based on a one-year volume commitment.
Toshiba America Electronic Components, www.toshiba.com

Image sensor uses wide-VGA format

Suiting intelligent-traffic systems, security and surveillance, and automotive-imaging systems, the KAC-00400 image sensor comes in a wide-VGA, 768×488-pixel format, providing 20% more pixels than standard VGA sensors. The expanded field of view provides additional data for pattern-recognition and object-detection algorithms. Additional features include a 60-frame/sec rate, a light-sensitive pixel, and a lower noise design for improved sensor imaging in low-light conditions. The KAC-00400 costs $15 (10,000).
Kodak, www.kodak.com

Frame-rate-converter IC generates 120 frames/sec

The FRC 94xyH high-definition frame-rate-converter IC generates 120 frames/sec from 50/60-Hz broadcast content and from 24-frame/sec film sources. Targeting full high-definition, 1920×1080-pixel digital televisions, the IC provides a processing resolution high enough to output the vendor's TruDHD HDTV. Available in a BGA-260 package, the FRC 94xyH costs $24 to $30.
Micronas, www.micronas.com

Power-stage IC forms core of Class D reference design

The CS44130 quad-power-stage IC forms the core of a Class D-amplifier reference design that targets 2.1-channel audio for digital TV and home-theater receivers. It provides as much as 60W of power and thermal and electrical self-protection. You can configure it as four half-bridge channels, two full-bridge channels, or one parallel full-bridge channel. It achieves system-level dynamic range greater than 105 dB. The IC comes in a 48-pin QFN package, and prices start at $2.78 (10,000).
Cirrus Logic, www.cirrus.com

Audio/video-component switch supports multiple formats

The TB1311AFG programmable audio/video-component switch accepts all standard analog-audio and -video signals for digital television, set-top boxes, and other audio/video products. You can configure the switch as 12-channel CVBS inputs, eight-channel Y/C inputs, four-channel YpbPr or RGB inputs, four-channel SCART inputs, two-channel video outputs, or a monitor output. The device has a left and right audio switch with 10 inputs and three outputs, a prefilter for the ADC, real-time format detection, automatic sync detection, and I²C-bus control. The price is $5 (10,000).
Toshiba America Electronic Components, www.chips.toshiba.com

Quad-channel decoder saves 25% in board space

The TVP5154 quad analog-to-digital video decoder accepts two composite inputs per decoder for a total of as many as eight camera inputs. The device converts NTSC, PAL, and SECAM formats to digital-video-output streams. It features four dedicated I²C addresses, which allow for as many as four TVP5154 devices, or 16 video chan-

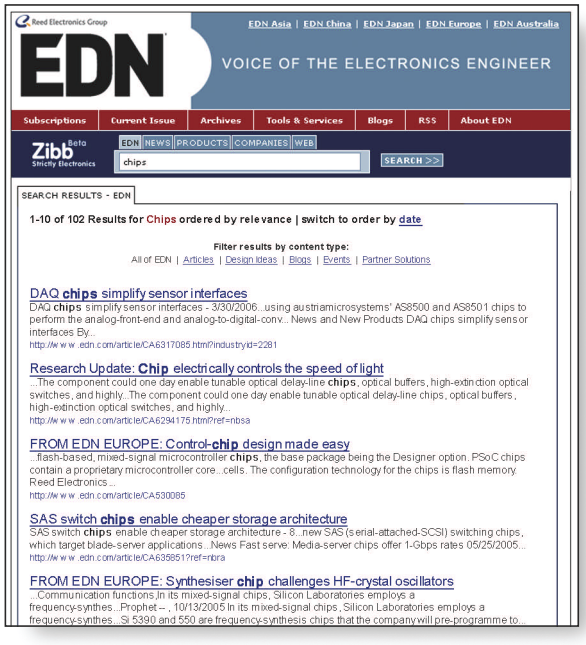


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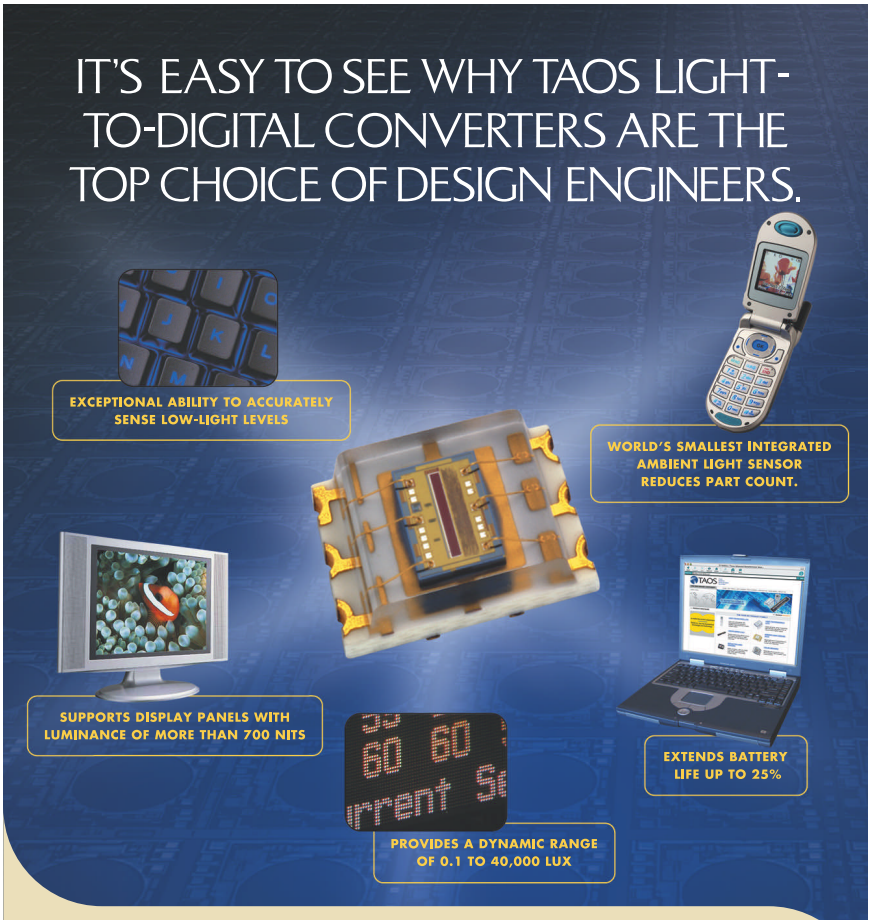
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Bright light or dim, indoors or out, the TAOS TSL2560/61 and the new low-voltage TSL2562/63 Light-to-Digital (LTD) Converters have what it takes to optimize display aesthetics and reduce eyestrain. Remarkably, battery life can also be extended up to 25% in a variety of mobile applications in which the display panel accounts for 30–40% of the total power consumption.

Using these LTD devices, the human eye response can be approximated over an effective 20-bit dynamic range with a 16-bit resolution without the use of an expensive photopic filter. Design-in time and cost is significantly reduced with these device's I²C (TSL2561/63) and SMBus (TSL2560/62) interfaces allowing them to be easily connected to a micro-controller where illuminance (i.e. ambient light level) in lux is derived. Additionally, no external circuitry is required for signal conditioning further reducing implementation cost. They can also be used for notebooks, tablets, flat-panel televisions, digital cameras, and mobile phones.

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nels, on a single I²C bus. The device comes in a 16×16-mm, 128-pin LQFP. The price is $9 (1000).
Texas Instruments, www.ti.com

Audio-capture IC targets portable digital-audio recording

The CS53L21 ADC IC provides high-quality audio capture for digital voice recorders, voice-recognition systems, digital microphones, and audio video-capture cards. An input multiplexer allows for switching between three stereo analog sources, followed by a programmable-gain amplifier with a gain range of 3 to 12 dB in 0.5-dB steps. The device also features an on-chip dual-microphone preamplifier and a programmable low-noise bias supply and allows independent control of the left and right channels' audio. It consumes less than 9 mW of power and supports a direct interface to logic levels of 1.8 to 3.3V. The device, which has a 98-dB dynamic range, comes in a 32-lead QFN package and costs $1.75 (10,000).
Cirrus Logic, www.cirrus.com

Satellite set-top-box decoder targets high-volume markets

The ST15188 satellite set-top-box receiver/decoder chip targets high-volume free-to-air markets in Asia, the Middle East, Africa, South America, and Europe. The device combines the functions of the vendor's STV0288 DVB-S receiver and STM5118 mass-market set-top-box decoder. The ST5188 integrates a QPSK (quadrature-phase-shift-keying) demodulator, audio DACs, and a voltage-controlled crystal oscillator. The device's software runs on a high-performance, embedded 32-bit ST20 RISC CPU core operating at 200 MHz. Available in a 176-pin, 20×20-mm QFP, the device sells for $4.50 (500,000).
STMicroelectronics Inc, www.st.com

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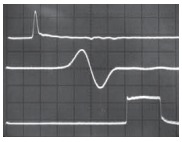
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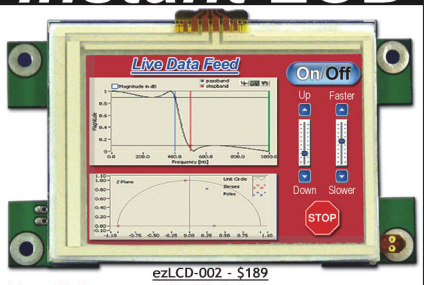
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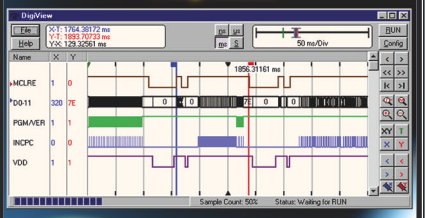
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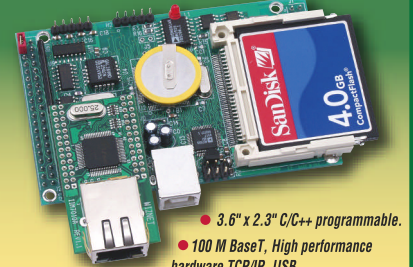
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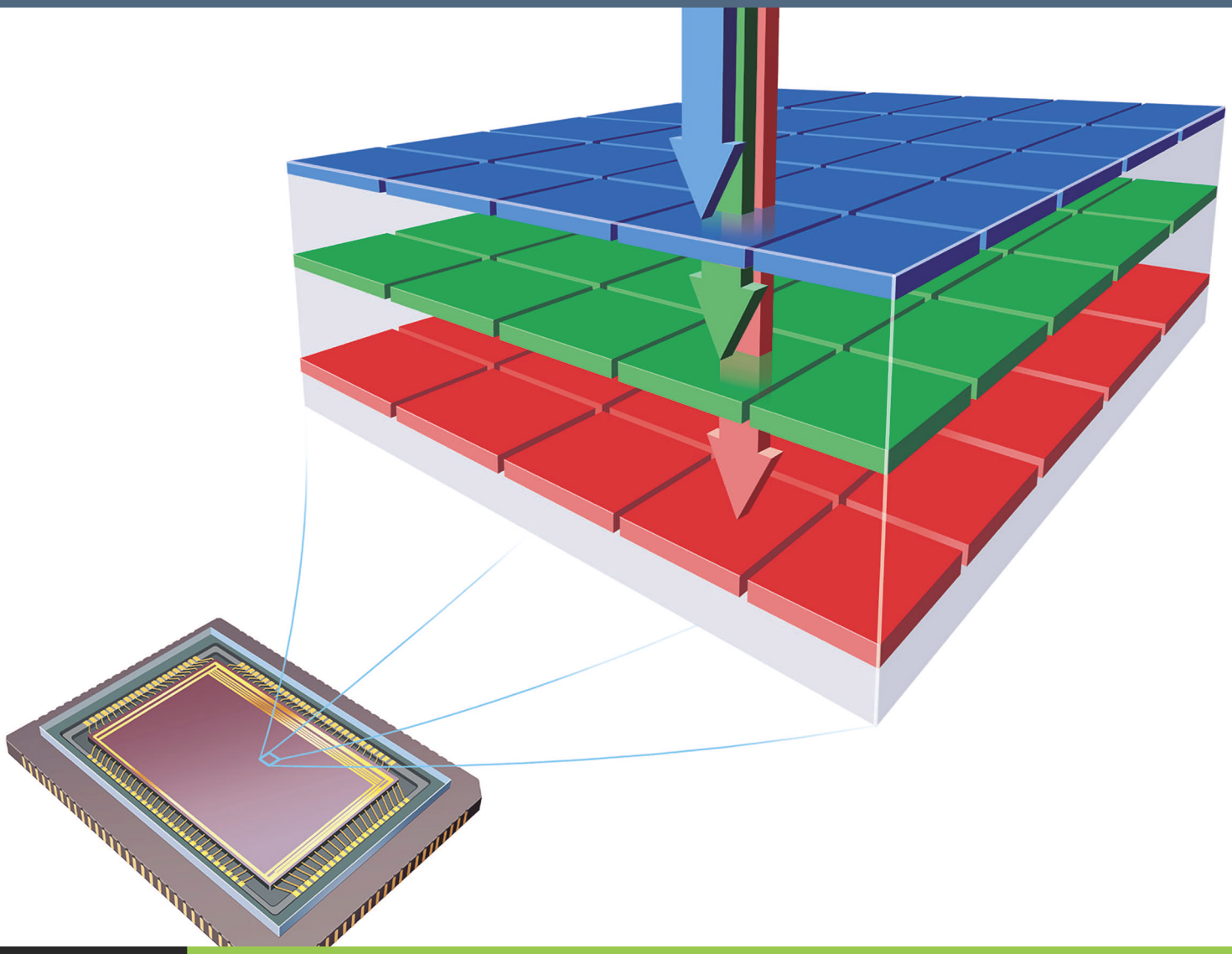
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Image sensor proves three can be less than one

Add Foveon (www.foveon.com) to the list of companies proving that elegant design does not guarantee commercial success. The company in 2000 unveiled its X3 image-sensor technology with fanfare and in 2002 delivered silicon. With a three-layer architecture capable of sampling red, green, and blue light at every pixel location, X3 promised sharper focus, truer colors, and fewer artifacts than conventional single-layer sensors, which sample only one color per pixel and require interpolation to fill in the rest. Foveon argued that, by eliminating interpolation, X3 would reduce bill-of-materials costs and win over camera makers.

To date, however, only five off-brand cameras employ X3 sensors. None of these has received glowing reviews, and one suffered a recall due to reported image-quality problems. "Users have seen no great distinction in the pictures generated by the three-layer sensor," says Paul Worthington, senior analyst with market researcher Future Image. Meanwhile, conventional CMOS sensors got cheaper and better, image-processing algorithms improved, and manufacturers refused to abandon their own sensor investments for an unproven technology. Today, Foveon has no chance of cracking either the consumer-camera market or the high-end segment, Worthington says. (Foveon did not respond to requests for comment.)—by Matthew Miller

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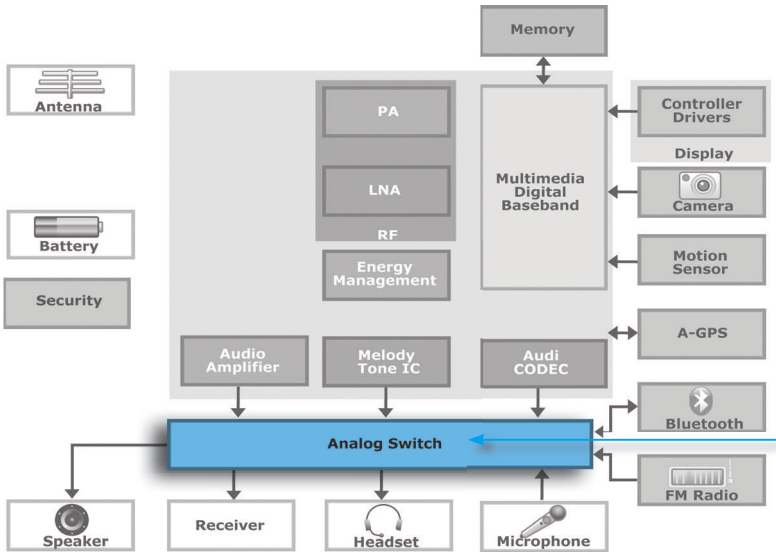
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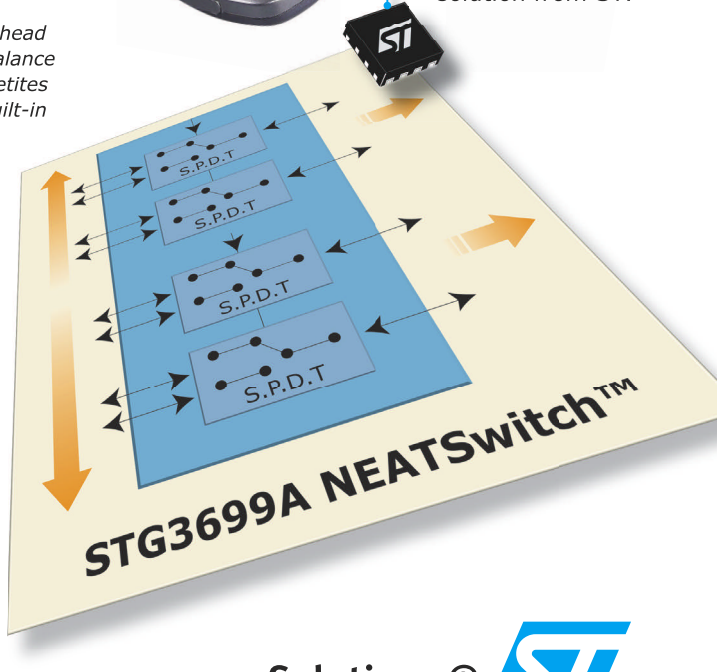
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